Practical Limits of Excimer Laser Lithography

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Outline

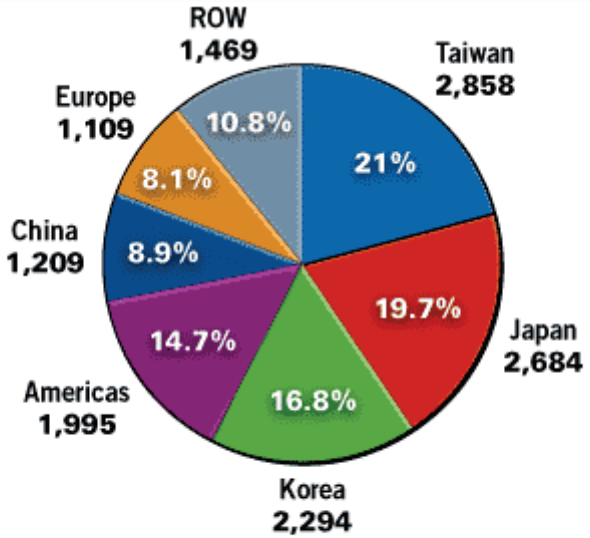
- Introduction:
  - About Author
  - About GLOBALFOUNDRIES
- Lithography Background
  - Focus on practical aspects of the Excimer Laser Lithography application in 28nm, 20nm and 14nm technology nodes
  - Up to 10B transistors Chip with feature size as tiny as 20nm are patterned using 193nm light… and all 10B need to work on SoC – how do we it?
- What is Excimer Laser Lithography
  - KrF scanner => ArF scanner => Immersion ArF scanner
  - Resist Materials
  - 3D transistors
  - Nanowires (wrap-around gate)
- Moore's Law – Twilight?
- LITHO Simulations from Dill ABC Model to PROLITH to SMO

H. Levinson et all. Lithography Target Optimization with Source-Mask Optimization. Proc. of SPIE Vol. 8326 83262P-1

2012 Top 10 Foundries

Top 12 2012 IC Foundries

2012F Rank	2011 Rank	Company	Four Ty					2012F Sales ($M)	2012/2011 Change (%)
1	1	TSMC	Pure-					16,720	15%
2	3	GlobalFoundries	Pure-					4,285	23%
3	2	UMC	Pure-					3,775	0%
4	4	Samsung	IDI					3,375	54%
5	5	SMIC	Pure-					1,625	23%
6	6	TowerJazz	Pure-					655	7%
7	7	Grace/HHNEC*	Pure-					605	7%
8	8	Vanguard	Pure-					590	14%
9	9	Dongbu	Pure-					540	8%
10	10	IBM	IDM	U.S.	430	420	-2%	435	4%
11	13	WIN**	Pure-Play	Taiwan	221	298	35%	425	43%
12	11	MagnaChip	IDM	South Korea	405	350	-14%	375	7%



Total capacity
13,618

Source: IC Insights

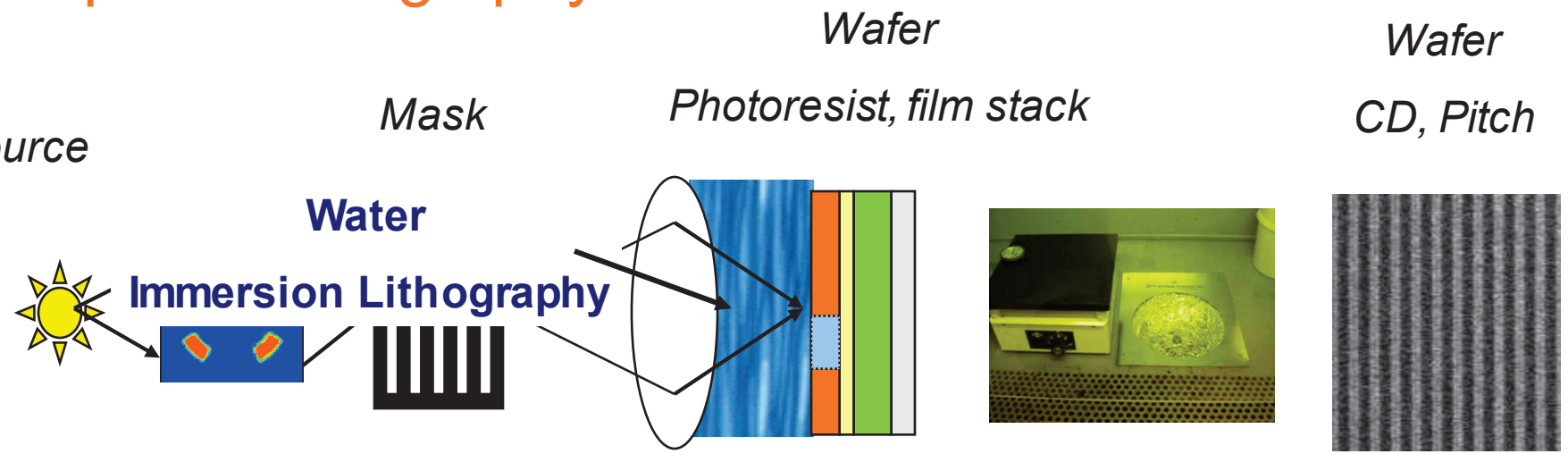
*Merged in 2012.
**GaAs foundry

Source: IC Insights, company reports

Excimer Laser Patterning– wavelength/10 resolution

- Focus on practical aspects of the Excimer Laser Lithography in 28nm, 20nm and 14nm nodes
- Up to 10B transistors SoC with feature size as tiny as 20nm are patterned using 193nm light… and all 10B need to work – how do we it?
  - Double Patterning
  - Triple Patterning
  - Reticles:
    - Phase-Shifting Masks
    - Attenuated Phase-shifting Masks
  - Illumination Schemes:
    - Off-axis Illumination
    - Customized Illumination (DOE)
    - Free Form Illumination

Optical Lithography



→ **NA_{lens} * n (1.43)**

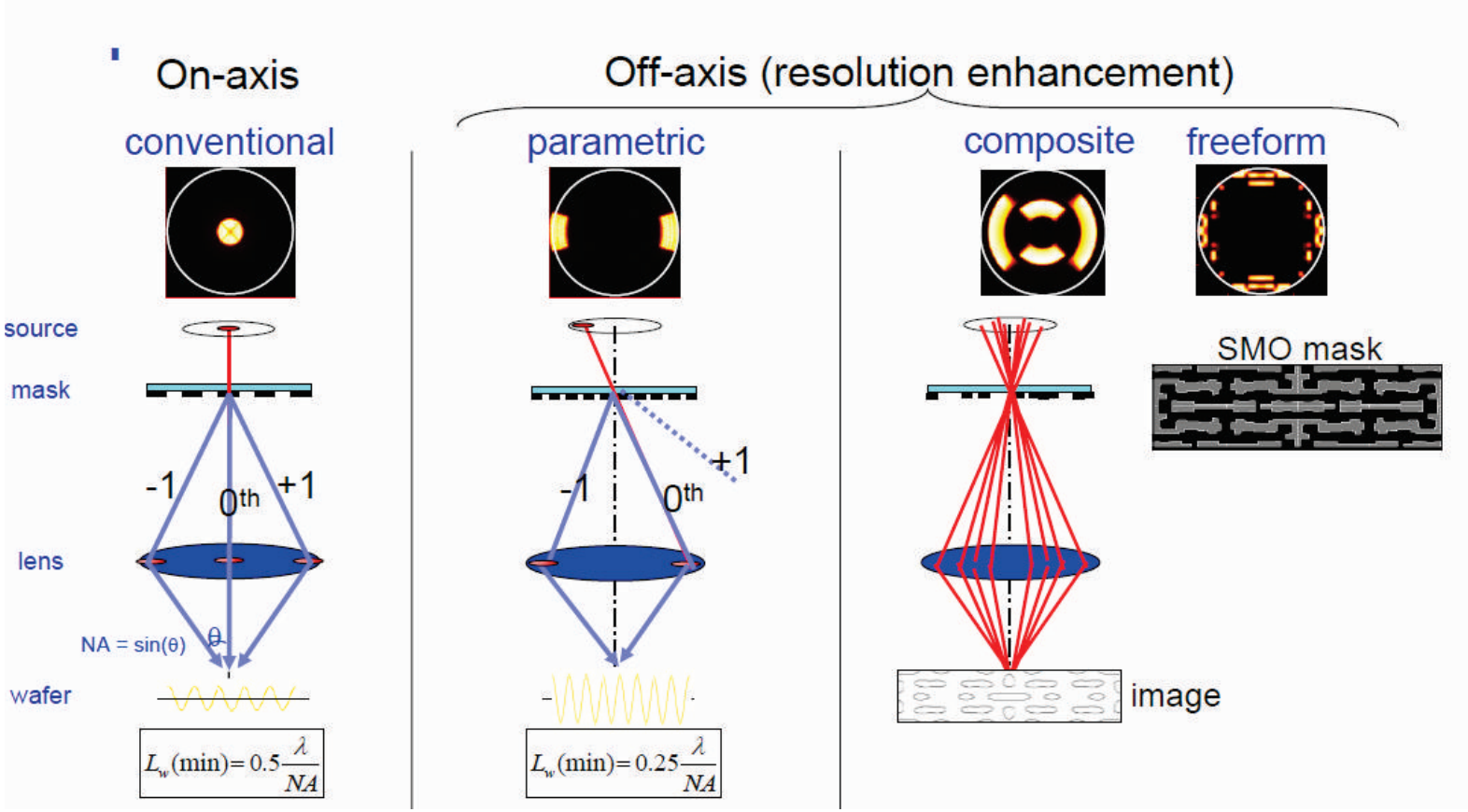
Resolution Limits:

$$P_{\min} \propto k_1 * \frac{\lambda}{NA}$$

k_1 fundamental limit of 0.25

CD_{min} limited by photoresist materials and process

Illumination Evolution: Pupil Shape



3-beam imaging

X-Y orientations equal

2-beam imaging

Double pitch

Improved 1-D imaging (X)

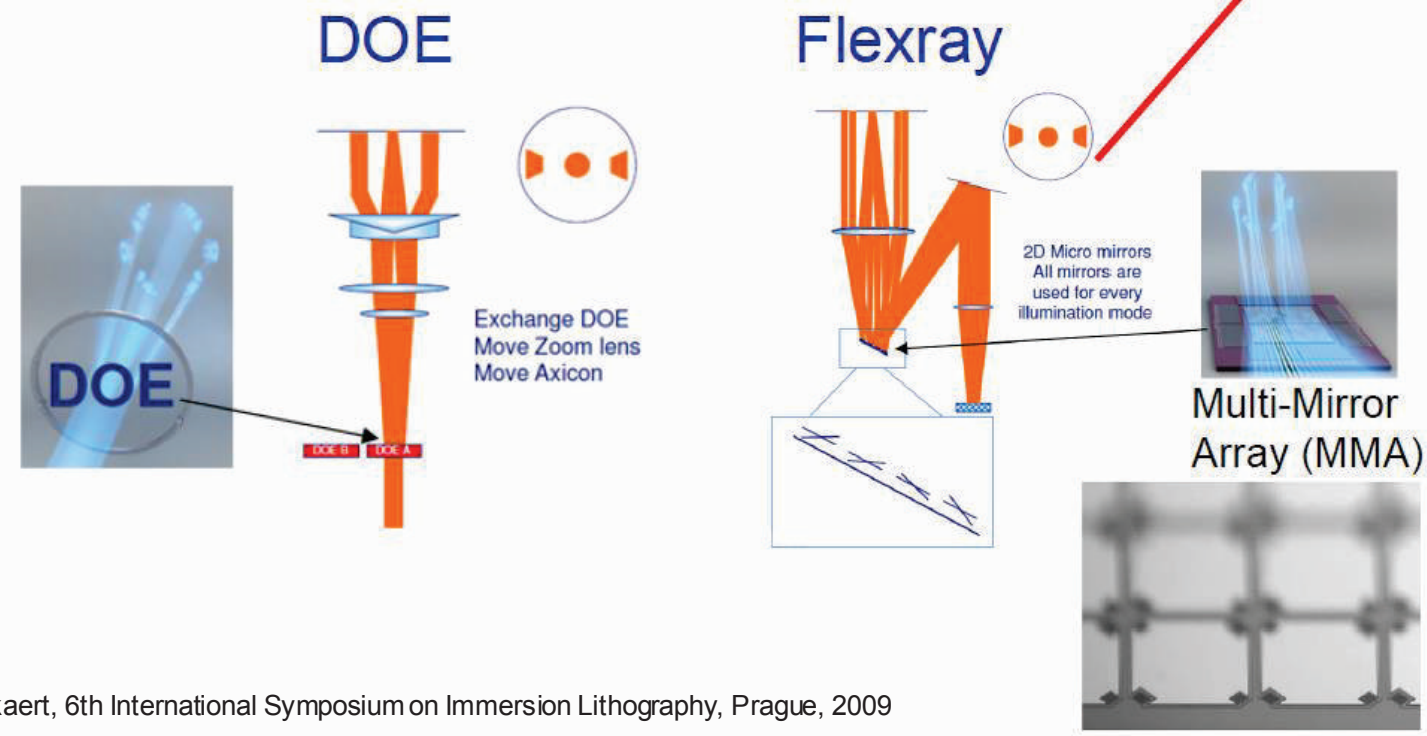
Multiple angle imaging

2-D optimization

SMO - Pupil and mask optimized together

Customized DOE and Programmable Illumination

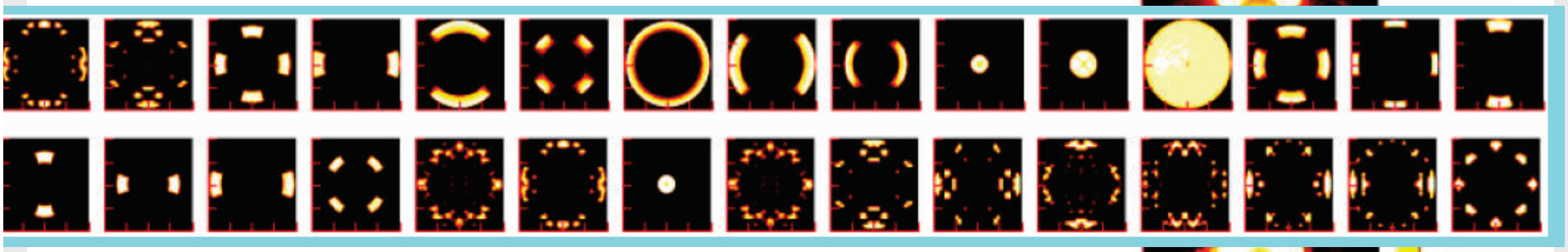
- Replaces diffractive optical elements (DOEs)
- Fully programmable illuminator based on multi-mirror MEMS array
- Initial focus of JDP was freeform DOE development



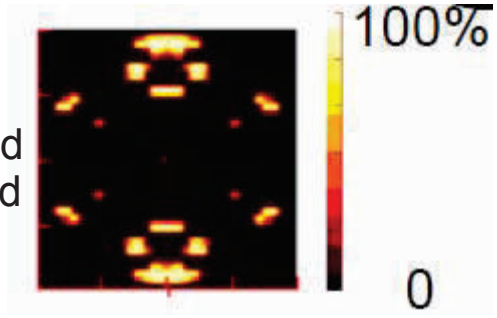
J. Bekaert, 6th International Symposium on Immersion Lithography, Prague, 2009

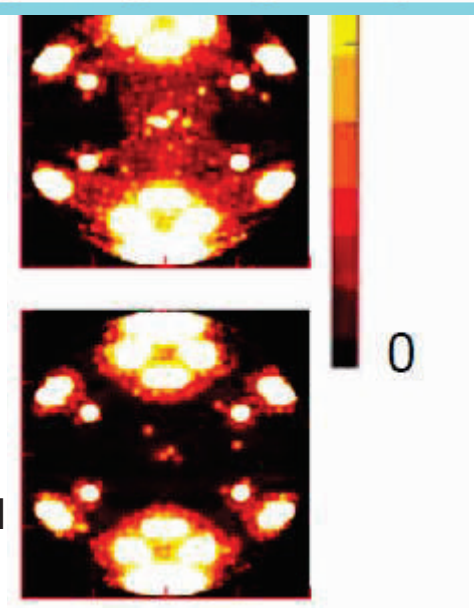
Programmable Source Benefits

- Save ~6-8wks in turn-around time for diffractive optical element (DOE)
- Instant creation of any pupil



- Less background stray intensity (sharper imaging)
- Better matching tool to tool
- Enables tool and mask specific source fine-tuning
- No change to user interface

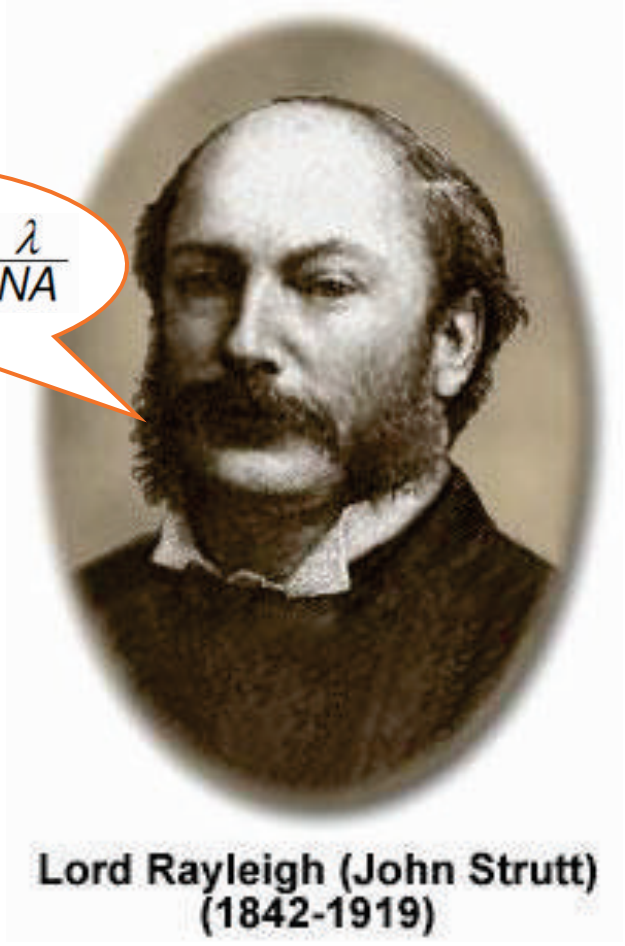




Device Scaling: Moore vs. Rayleigh

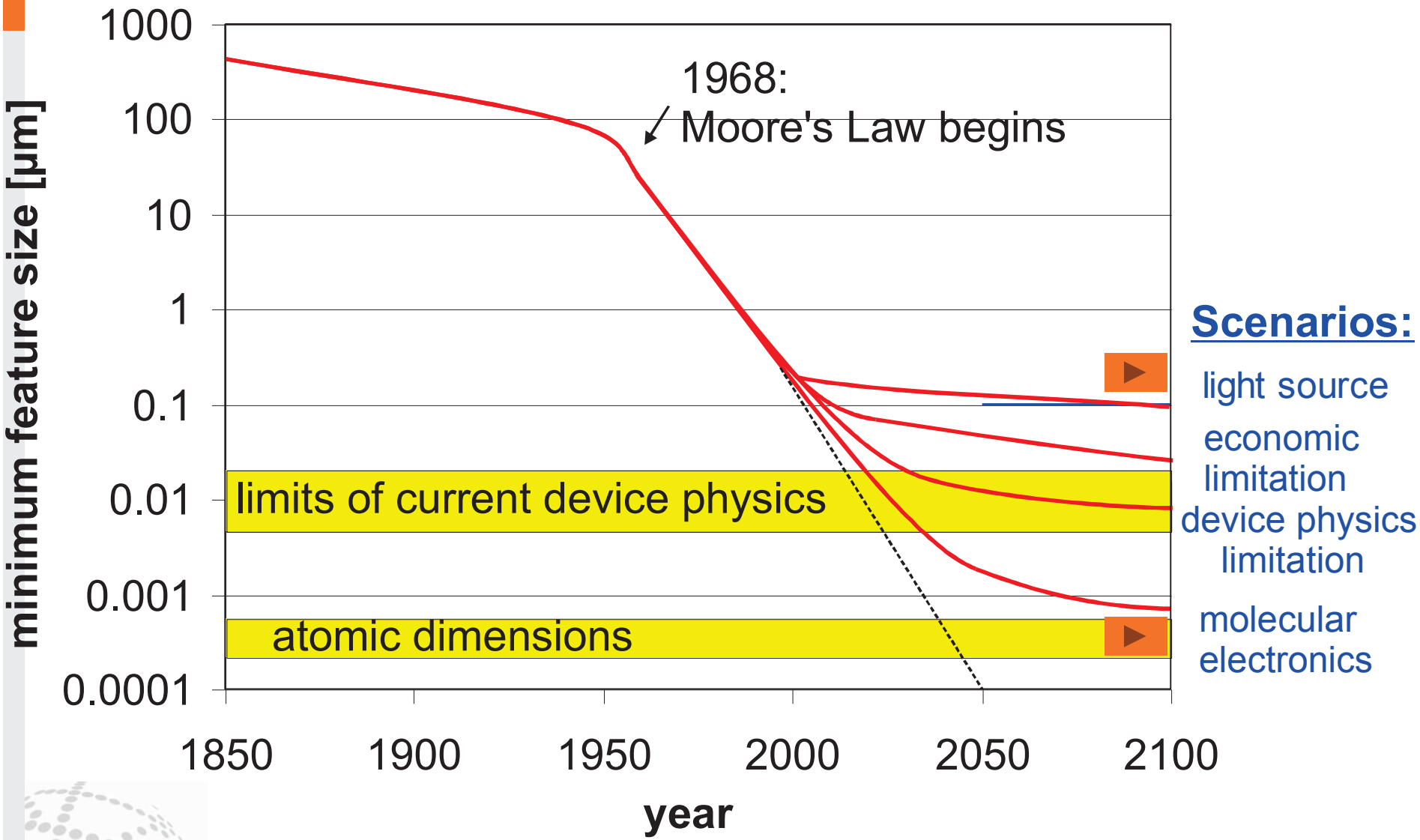
http://www.nature.com/news/2005/050421/images/moore.jpg

$$Resolution = k_1 \times \frac{\lambda}{NA}$$

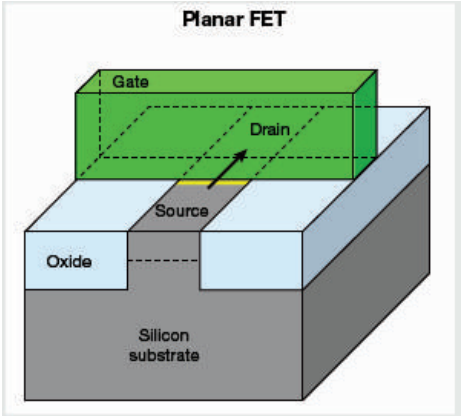


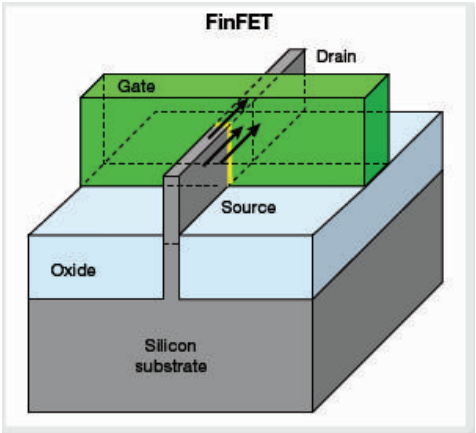
http://en.wikipedia.org/wiki/John_William_Strutt

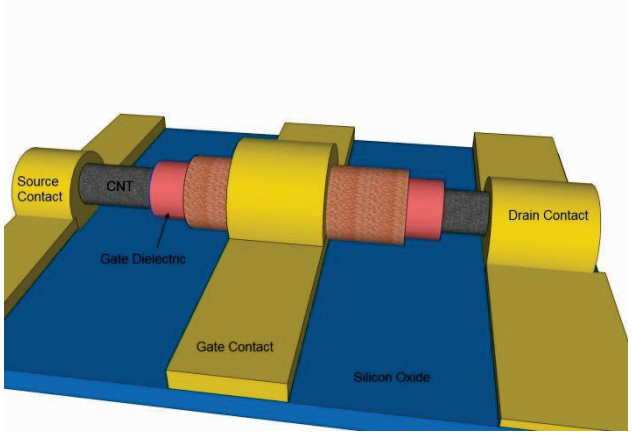
Moore's Law – When will it end?



3D-MOSFET



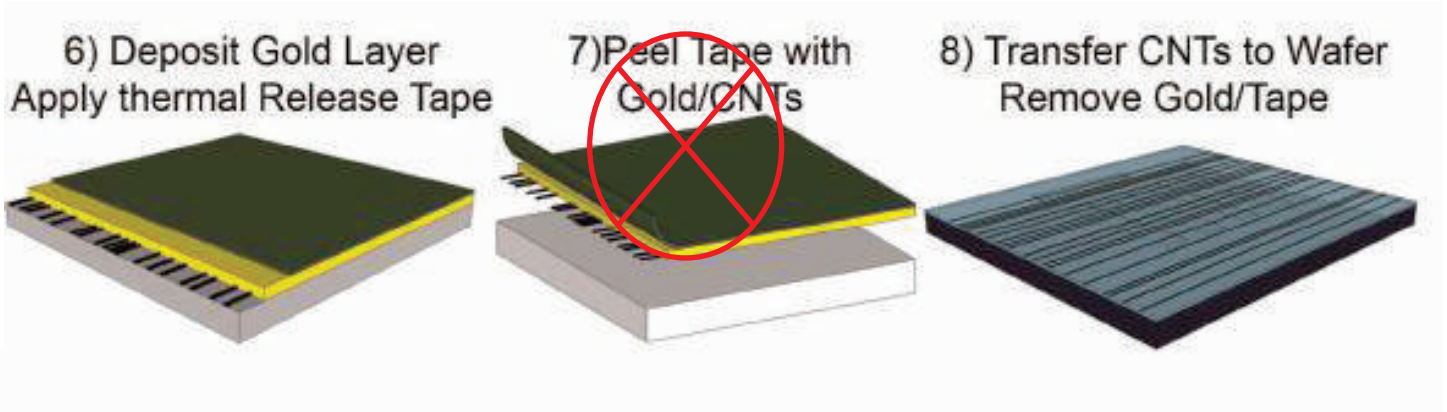




32nm min feature

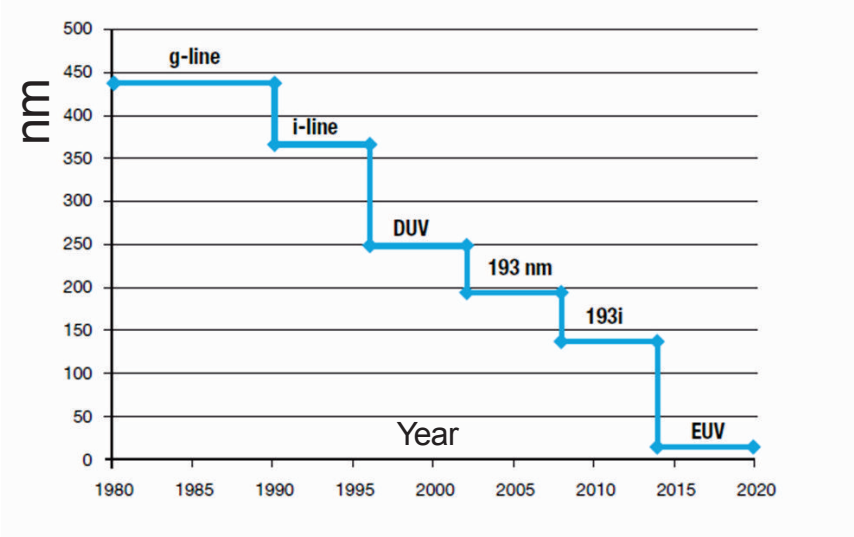
20 nm min feature

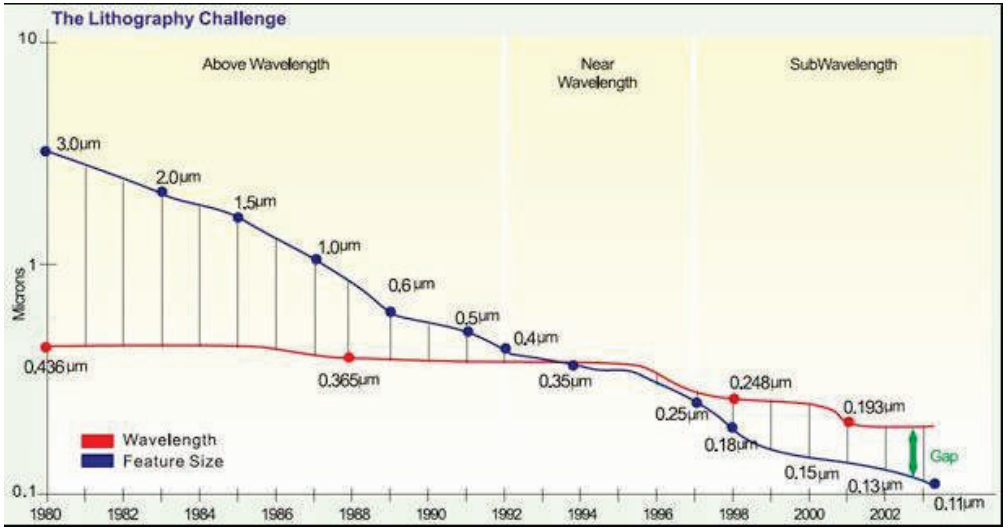
10 nm min feature



Light Source Evolution: Shorter Wavelength

Light Source		Wavelength nm
Mercury Arc Lamp	g-line	436
	h-line	405
	i-line	365
Excimer Lasers	KrF	248
	ArF	193
DPP or LPP	EUV	13.5

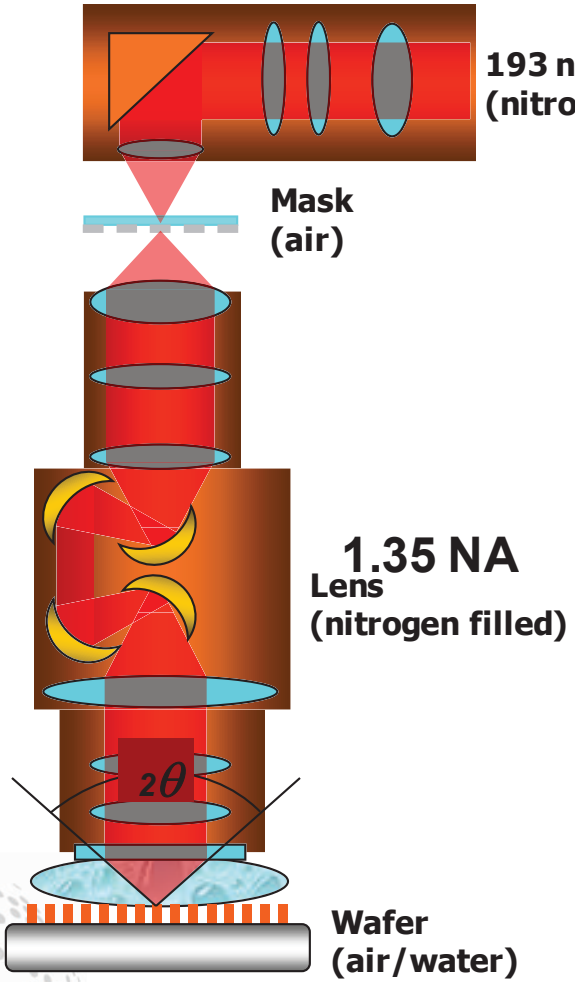




M. Preil, Future Fab International, Issue 38, 2011

Modern 193 nm ArF Lithography Tool

ArF Immersion Scanner Schematic



ASML 193 nm TWINSCAN Immersion

λ = 193 nm NA = 1.35

$$HP = k_1 \lambda / NA$$

Excimer Laser – Fab Abatement

XLA-300 Cymer 193nm Laser

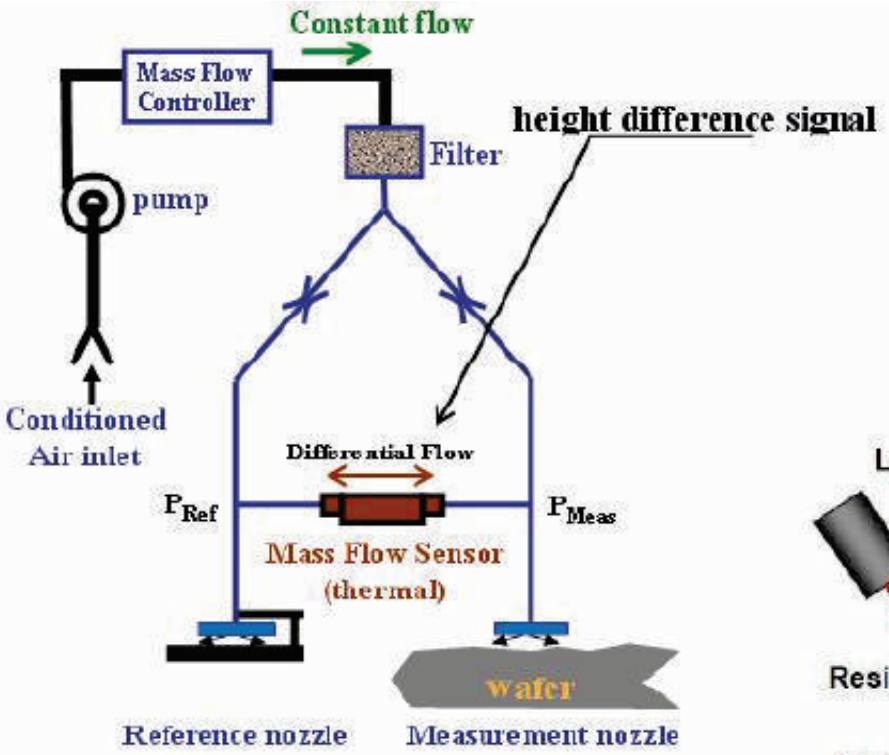
Top Level Specification

Rep Rate, Energy and Power		
Power	W	90
Operational Energy Range (Total Range)	mJ	10.0 - 15.0
Rep Rate Range (OTS applies)	kHz	1.5 - 6.0
Pulse duration (TIS)	ns	≥ 72
Duty Cycle	%	75
Spectral Characteristics		
FWHM	pm	0.12
E95%	pm	0.25
E95% BW Stability	pm	0.05
ASE		<3 10-4
Energy/Dose Stability		
Dose stability	%	≤ +/- 0.10

Model	Rep. rate	Fan Power
XLA-300	6000Hz	5600 W

W. Gillespie , Proc. of SPIE Vol. 5754, p. 1293

Immersion Scanner –Agile Intra-field Leveling



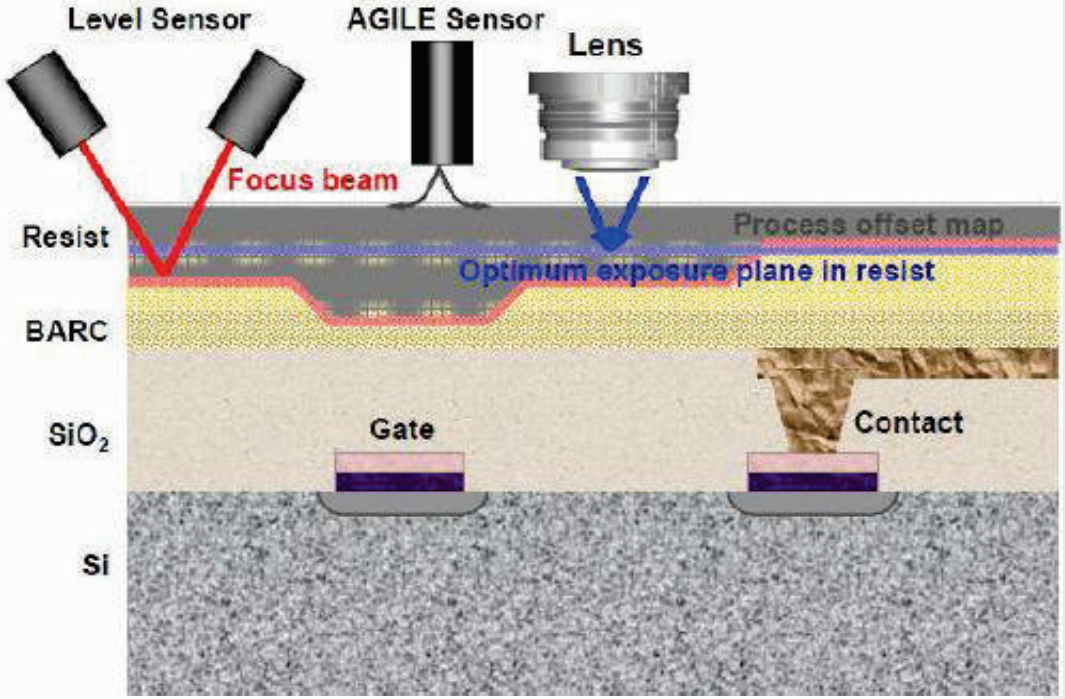
AGILE:

The AGILE application uses the AirGauge focus sensor in order to measure the top surface of the resist.

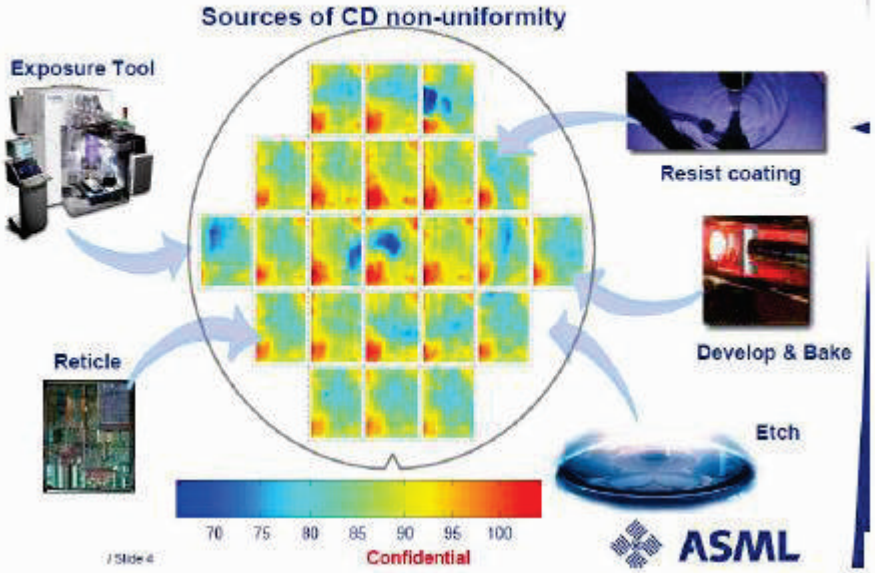
In combination with the level sensor wafer map the AGILE application ensures optimal leveling and productivity on process wafers

Improvements observed up to 50% reduction in focus variation across field

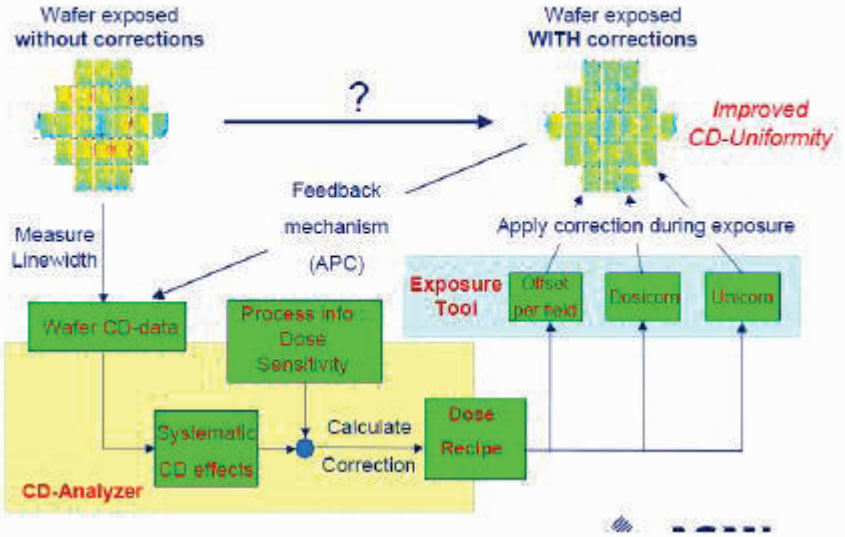
Fab1: 100% fields measurement initially for 1-2 wafer in a lot per Device, per Layer, per Scanner. Thereafter, APC update annually using 13 fields/1 wafer/x number lots Sample plan.



CD Uniformity (CDU)

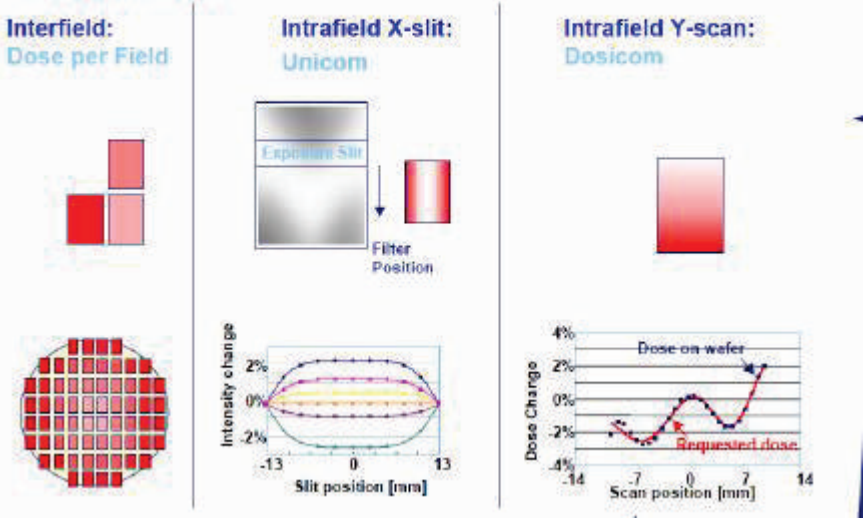


DoseMapper concept



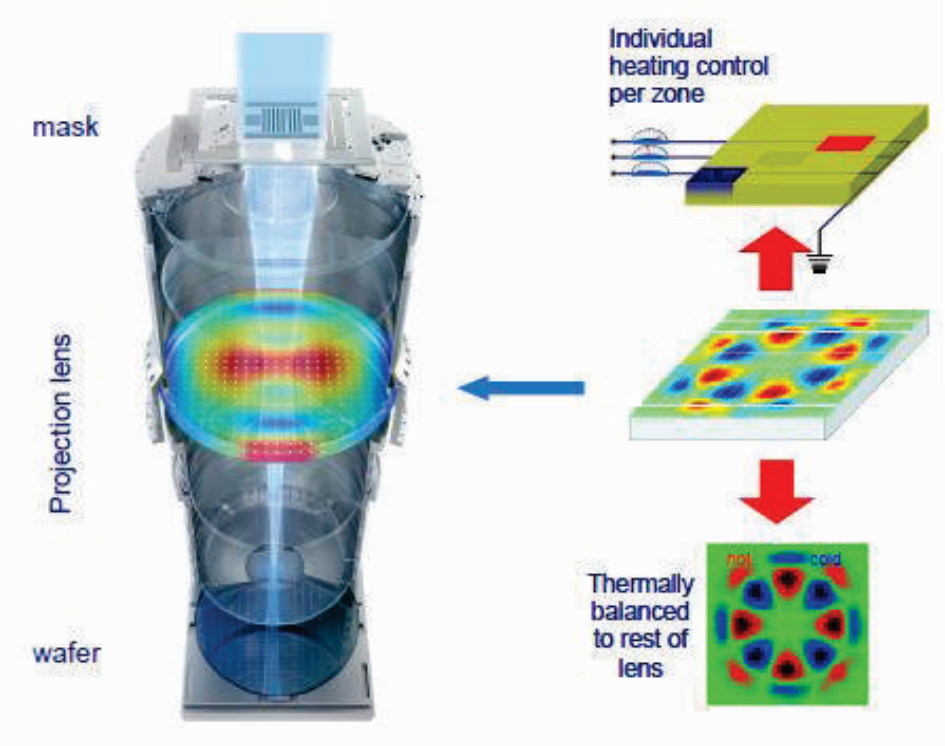
DoseMapper concept

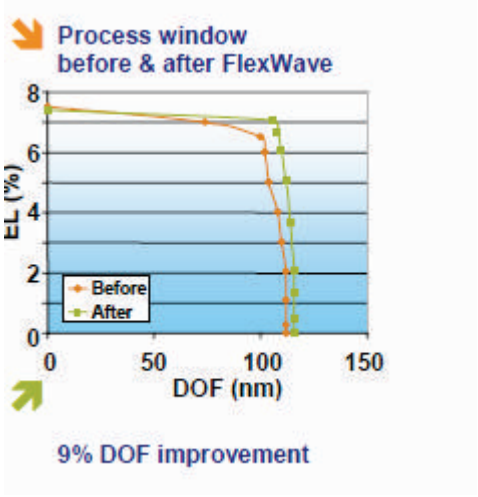
Dose actuators

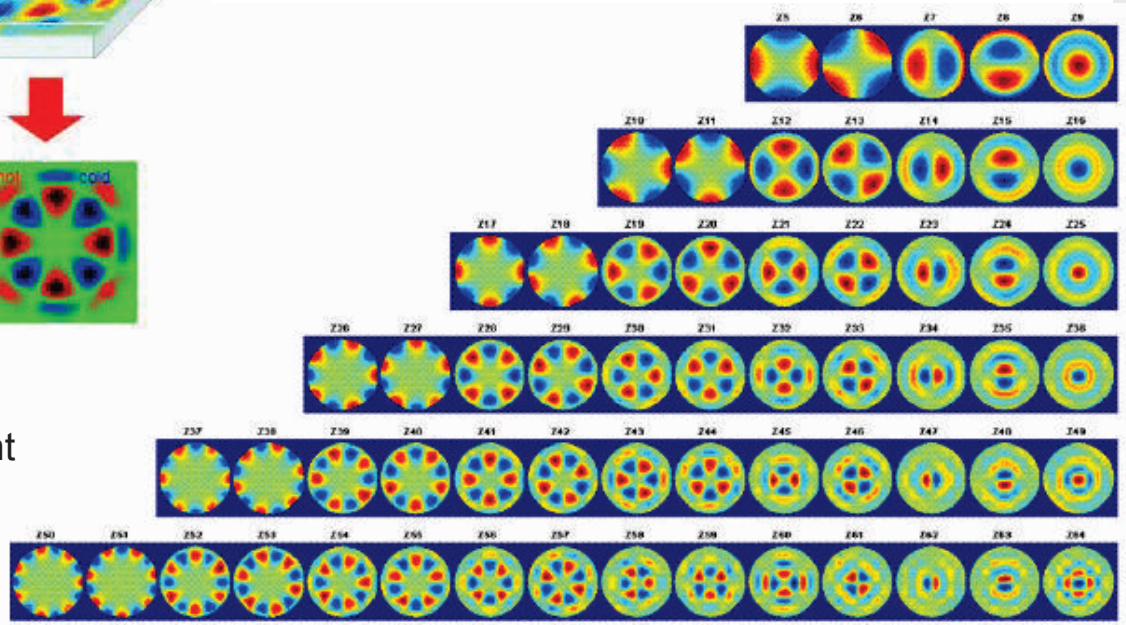


- **Inter-field Errors**
  - **Dose Correction**
- **Intra-field Errors**
  - **Slit Exposure Correction**
  - **Scan Exposure Correction**

Advanced Wavefront Engineering





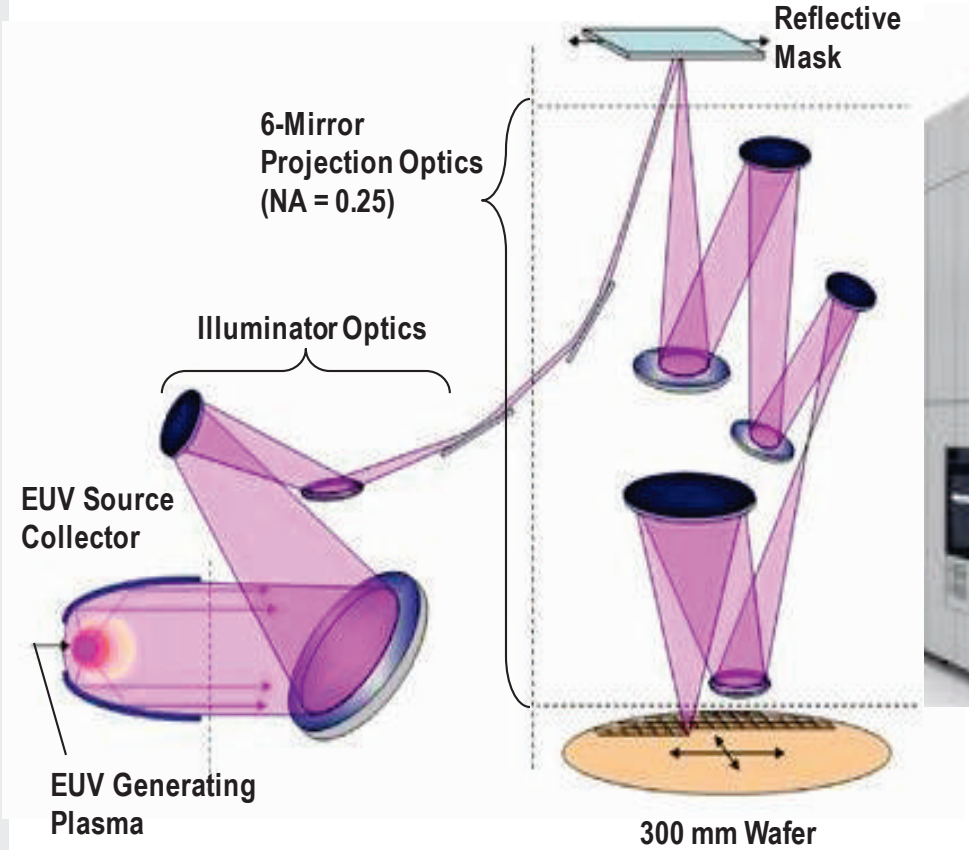


Principle of the FlexWave an optical element close to a pupil plane of the projection lens with heating zones

F. Staals et al. Proc. of SPIE Vol. 7973, 2011

Extreme Ultraviolet (EUV) Lithography Tool

EUV Projection Optics Schematic



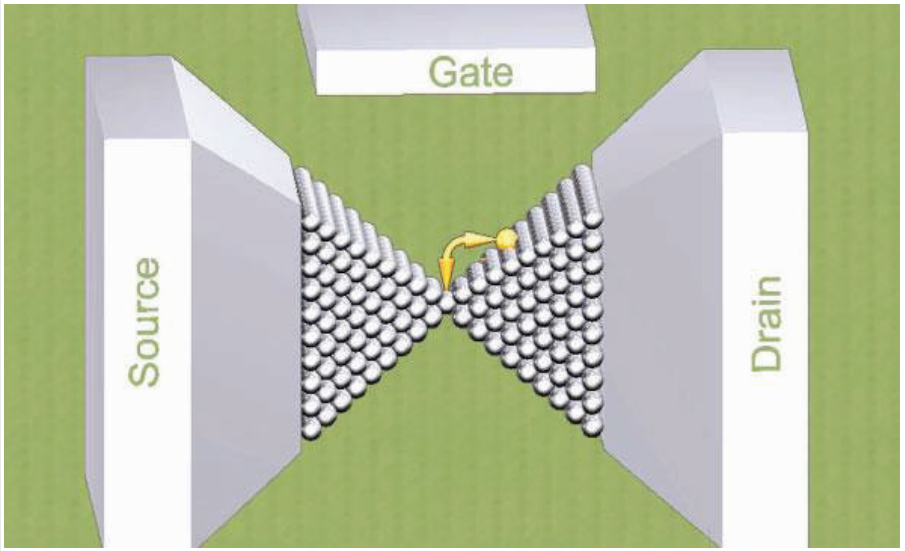
ASML 13.5 nm NXE:3300B Scanner

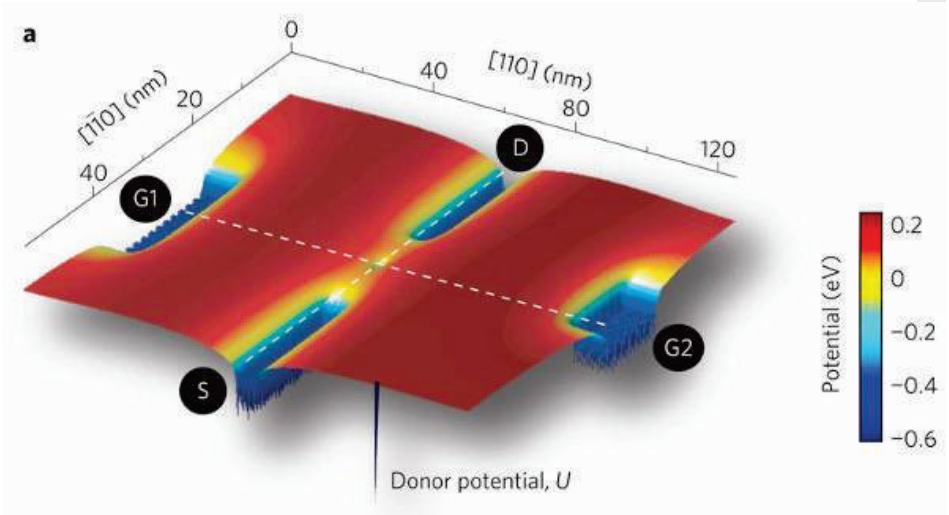
λ = 13.5 nm NA = 0.33

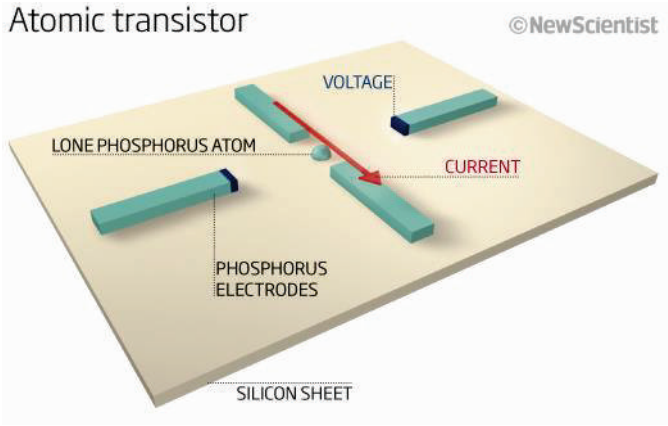
$$HP = k_1 \lambda / NA$$

Ref: S. Wurm (SEMATECH)

Single Atom Transistor

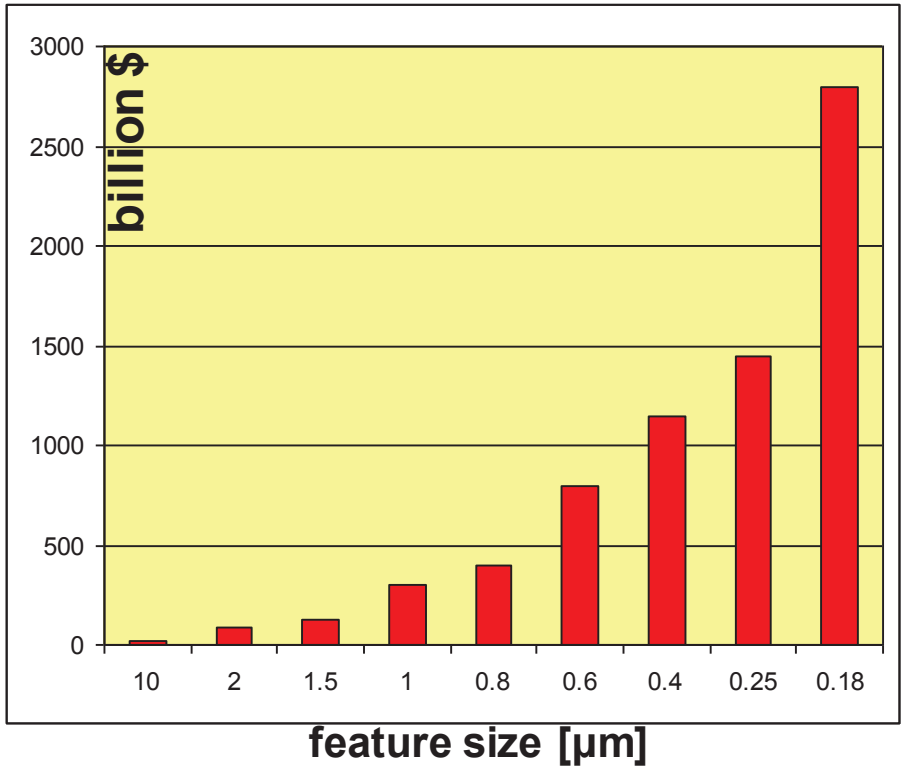


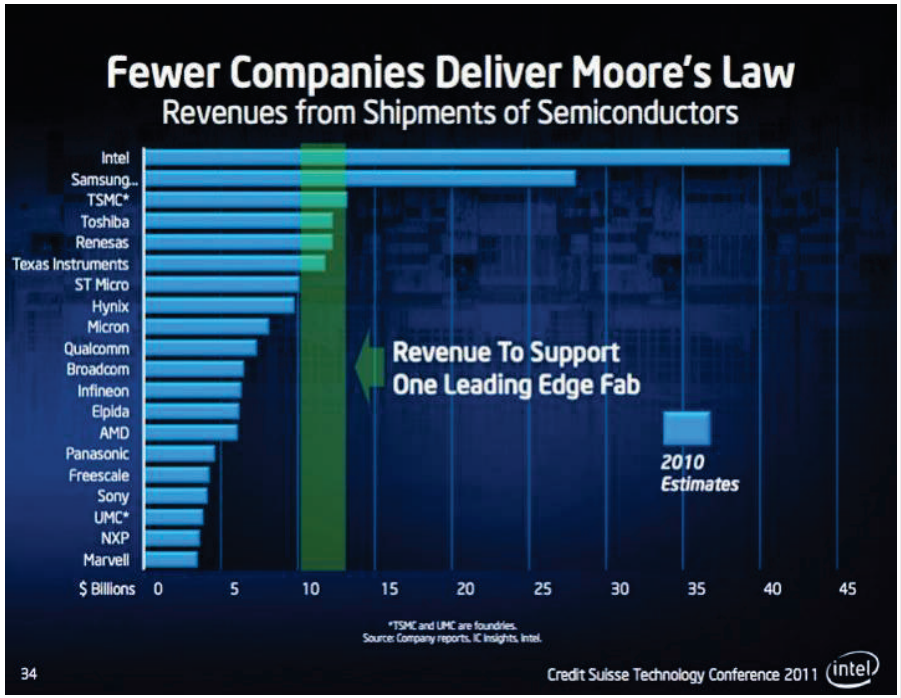




M. Fuechsle et al. Nature Nanotechnology, V 7, pp 242–246, 2012

Cost of Wafer Fab As a Function Of Feature Size

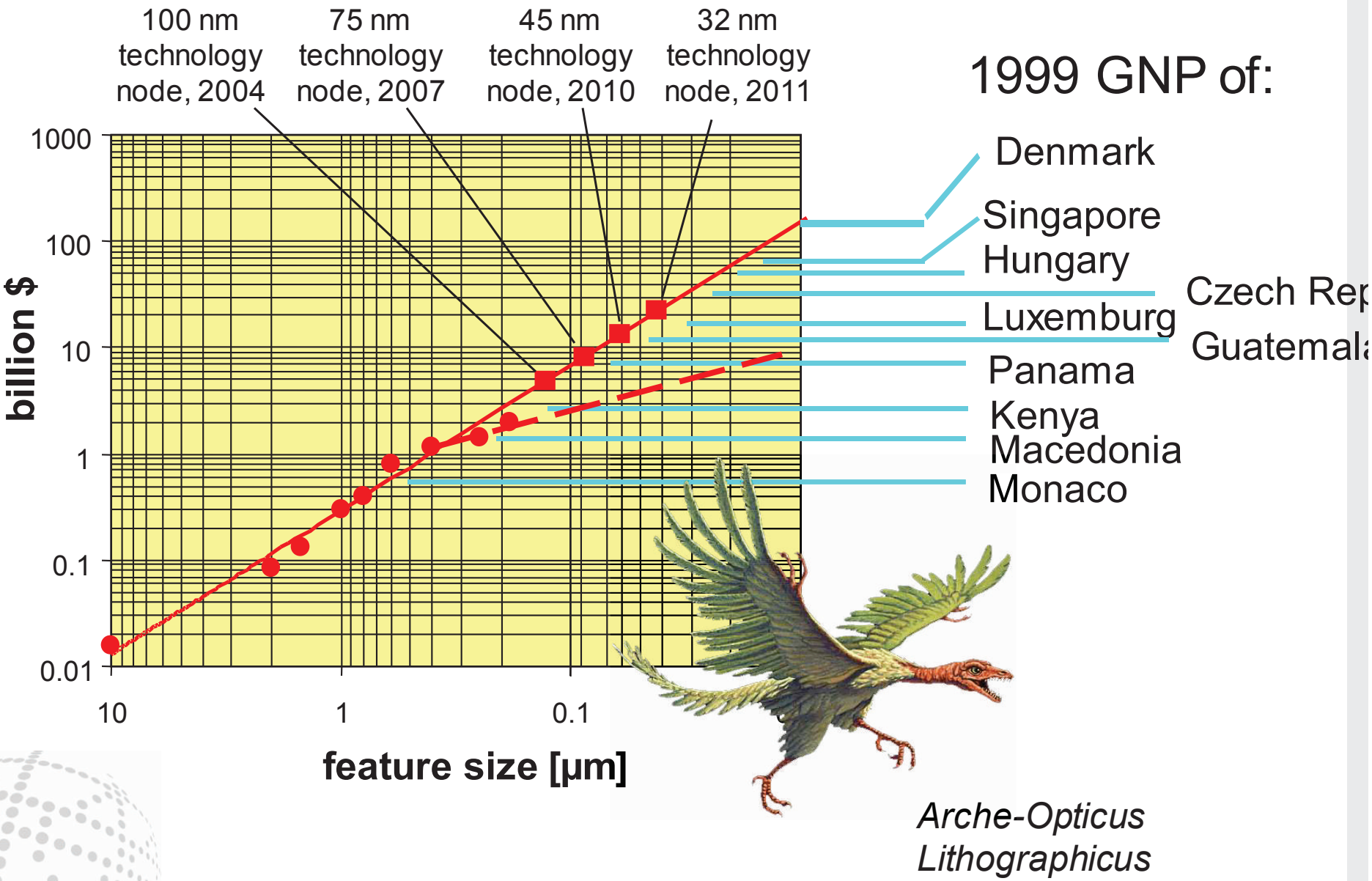




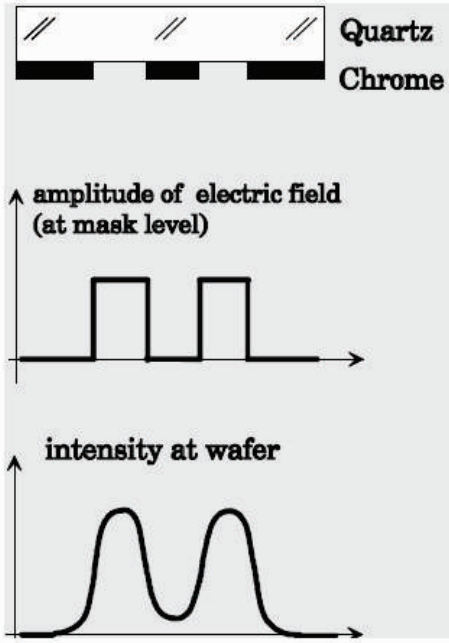
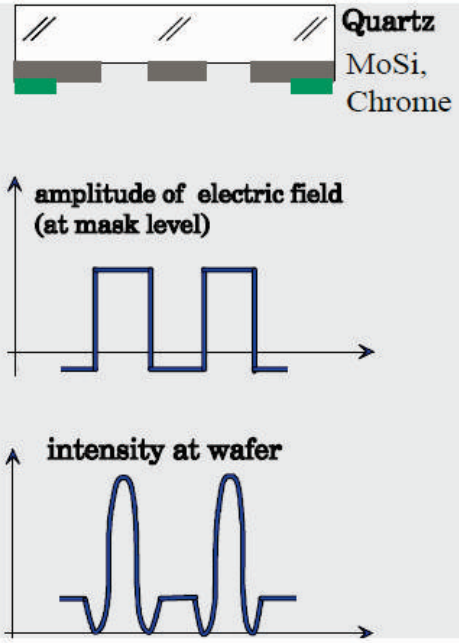
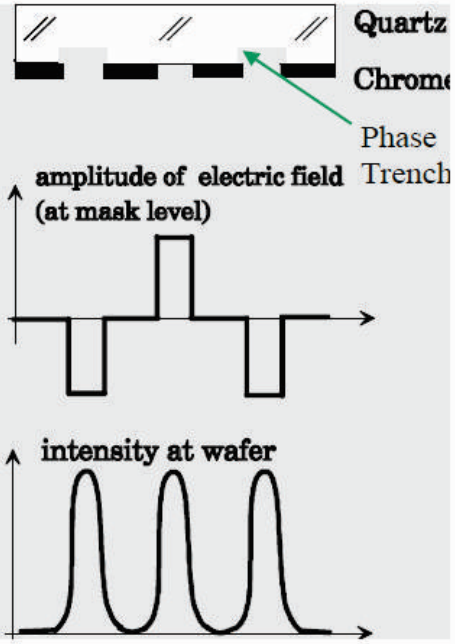
Economics of Moore's Law: in XX Century

...and in XXI Century!

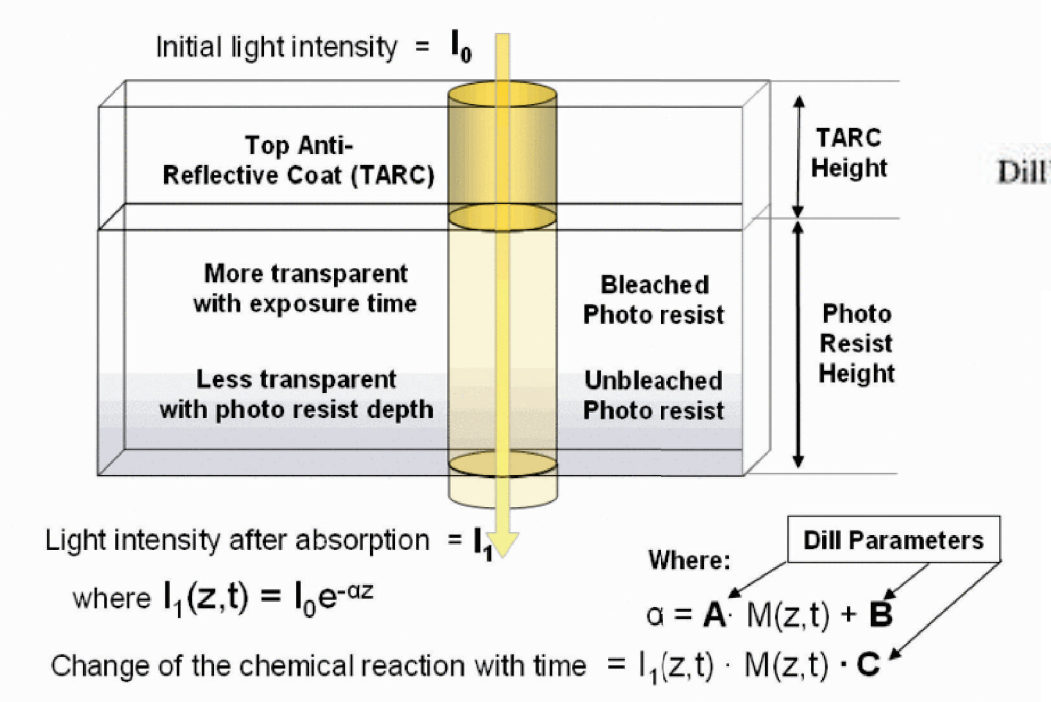
Rising Cost of Wafer Fab vs. GNPs



Reticles for Excimer Laser Litho

Conventional Chrome (COG) & OMOG	Half Tone Phase Shift (EAPSM)	Alternating Phase Shift (AAPSM)
		
Benefit: Lower cost of process; Thin mask model for advanced 32nm work. Application: Implants, and new Binary OMOG variants • WOG - 32nm Critical • WOH 28 nm Critical • W4F for 20 nm planned but ABF2 possible	Benefit: Enlargement of process latitude in lithography; small improvement of resolution. Application: Levels with contact-holes or similar structures.	Benefit: Better resolution, enlargement of process latitude & DOF in lithography; Application: Poly / Contact /– Not used at this time

Dill Model



For G-line, I-line novolak resists

Dill's equation for the imaginary refractive index k is

$$k = \frac{\lambda}{4\pi}(Ae^{-CE} + B). \qquad (1)$$

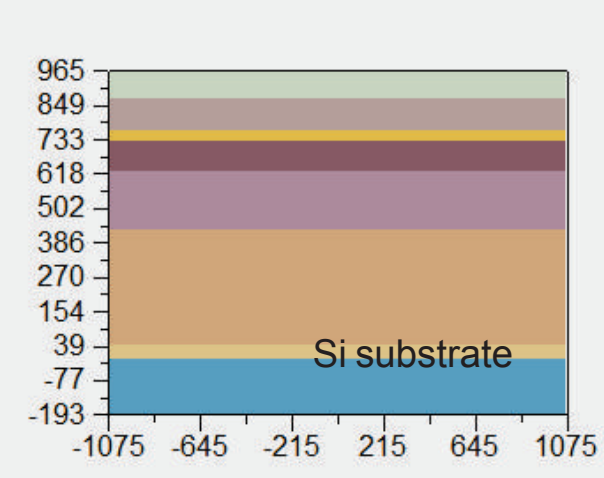
Modification of Dill Model for Chemically Amplified Resists

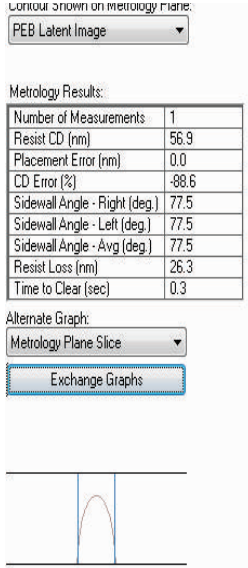
$$k = \frac{\lambda}{4\pi}(Ae^{-CE} + B)_{rising} + \frac{\lambda}{4\pi}(A_f e^{-C_f E} + B_f)_{falling} \qquad (2)$$

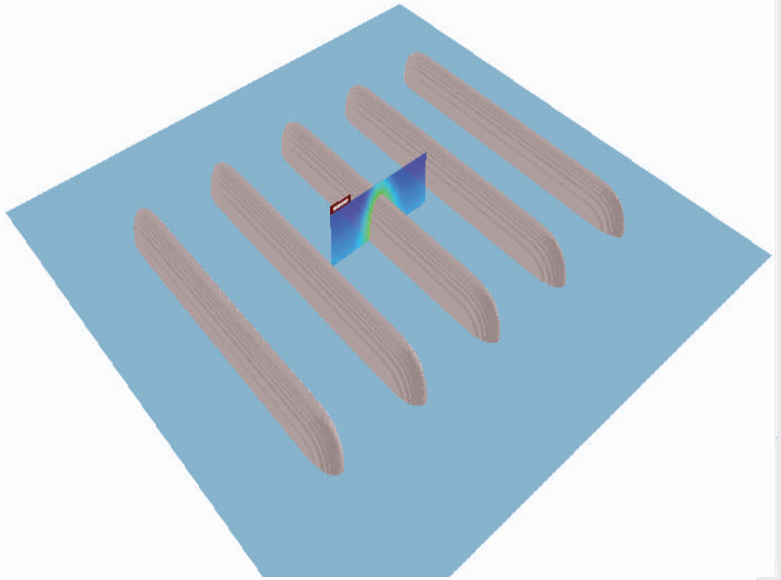
S.K. Kim "Exposure Simulation Model for CAR. Optical Review, Vol .10, Issue4, pp335-338

PROLITH

E. Barash, S. Randhawa. *Proc. SPIE* 3183, Microlithographic Techniques in IC Fabrication, 82 (August 14, 1997);



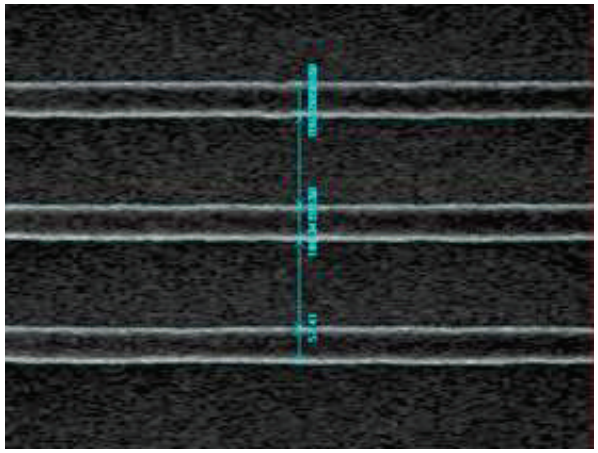




Step	Type	Name	Thickness (...
8	Coat	TCX041	90.000
7	Resist	TOK TArF Pi6-001ME (F...	105.000
6	Coat	A940 SiARC	35.000
5	Deposit	ODL-HM8014	100.000
4	Deposit	Si Dioxide	200.000
3	Deposit	Si Nitride	385.000
2	Deposit	Si Dioxide	50.000

Wafer Processes

Process 8: TCX041 (coat)	
Thickness (nm)	90
Refractive Index (real)	1.52
Refractive Index (Imaginary)	0.007
Process 7: TOK TArF Pi6-001ME (	
Thickness (nm)	105
Process 6: A940 SiARC (coat)	
Thickness (nm)	35
Refractive Index (real)	1.64
Refractive Index (Imaginary)	0.15
Process 5: ODL-102 (deposit)	
Thickness (nm)	100
Refractive Index (real)	1.5
Refractive Index (Imaginary)	0.3
Process 4: Si Dioxide (deposit)	
Thickness (nm)	200
Refractive Index (real)	1.56312
Refractive Index (Imaginary)	0
Process 3: Si Nitride (deposit)	
Thickness (nm)	385
Refractive Index (real)	2.66348
Refractive Index (Imaginary)	0.24013
Process 2: Si Dioxide (deposit)	
Thickness (nm)	50
Refractive Index (real)	1.56312
Refractive Index (Imaginary)	0
Process 1: Silicon (substrate)	
Refractive Index (real)	0.883143
Refractive Index (Imaginary)	2.77779



Integral Part of Design Flow

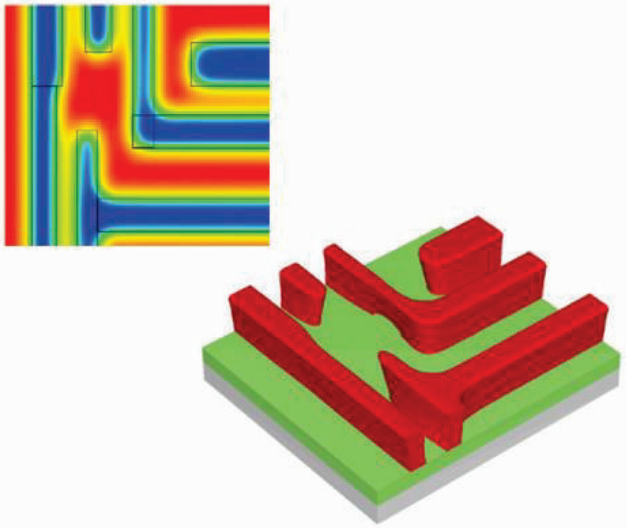


Figure 1: The importance of resist simulations in three dimensions: (*left*) aerial image and (*right*) photoresist as patterned on wafer with undercut.

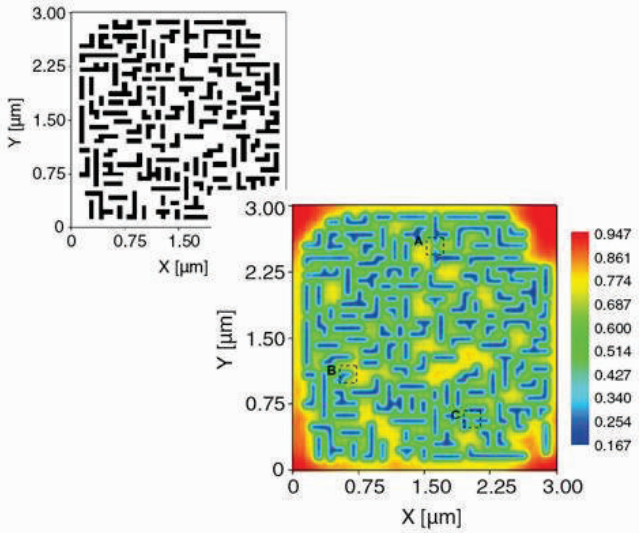
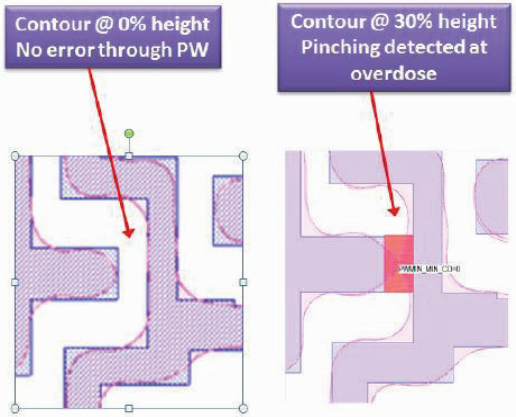
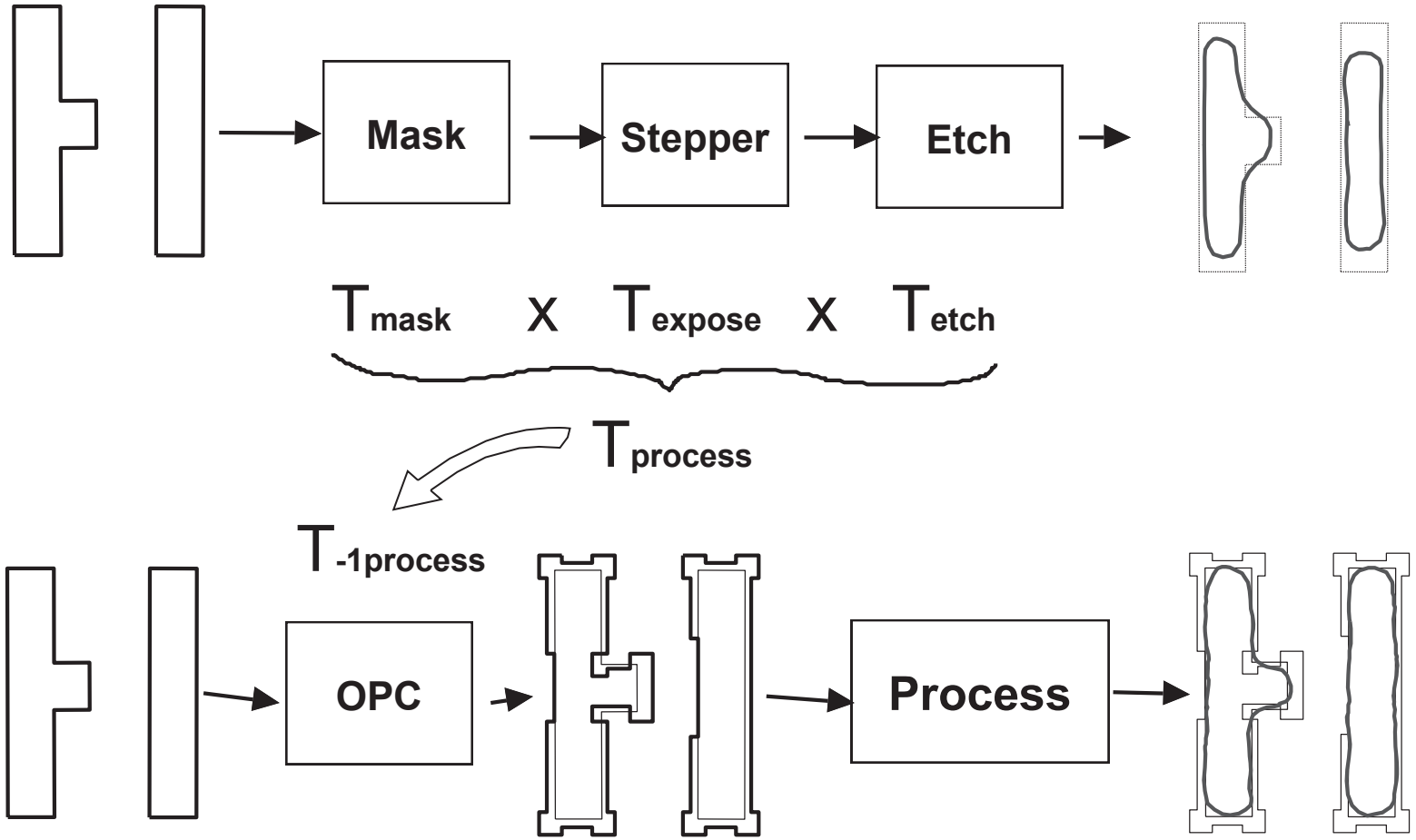


Figure 2: Simulation results for a large topographic mask area: (*left*) sample layout 3 x 3 µm^2, 3D mask and (*right*) aerial image intensity.



Y. Fan et al. Proc. of SPIE Vol. 8683 868318, 2013.

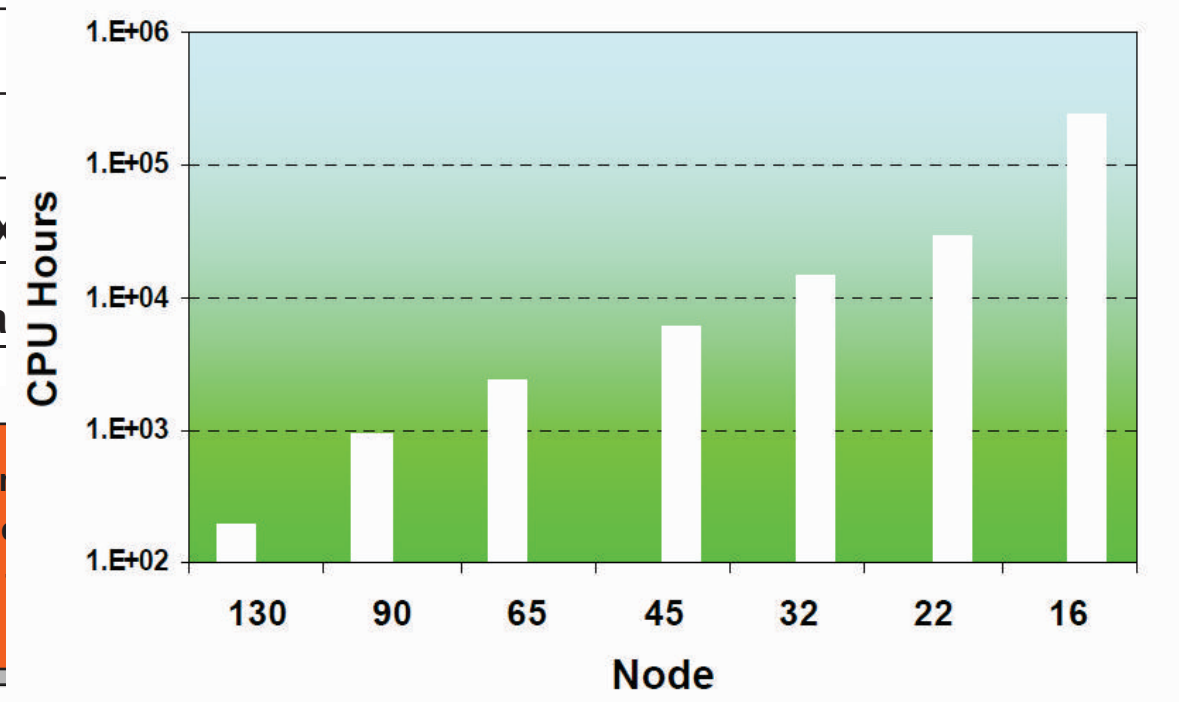
Optical Proximity Correction (OPC)



Technology Requirements and Greater Dependence on Simulations

Node, Year	90nm	65nm	45nm	32nm	22nm	15nm
Pitch	250nm	200nm	140nm	100nm	~70nm	~50nm
λ	193nm					
NA	.75					
tool scaling	85%					
Patterning Solutions	Optical Prox off a					
Edges	600 M					
Computational Needs(CPUs)	100	200	300	500	1000	2000

- Each edge placer
- Tolerances get v
- Process latitude
getting smaller.

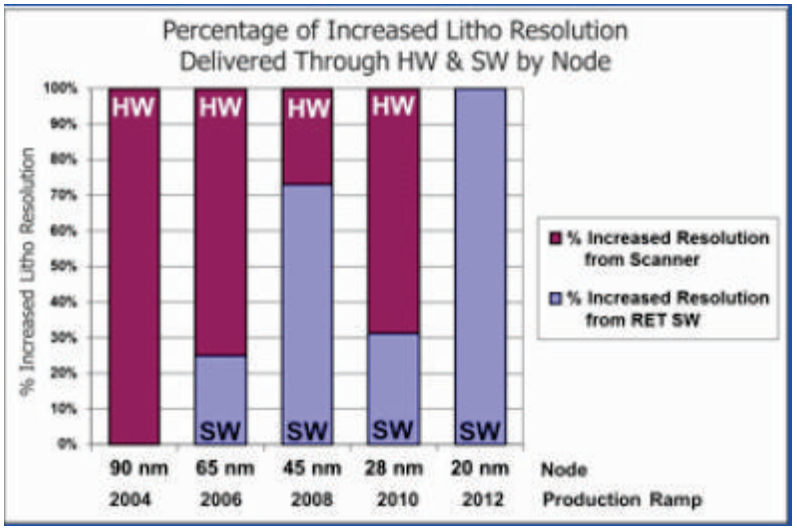


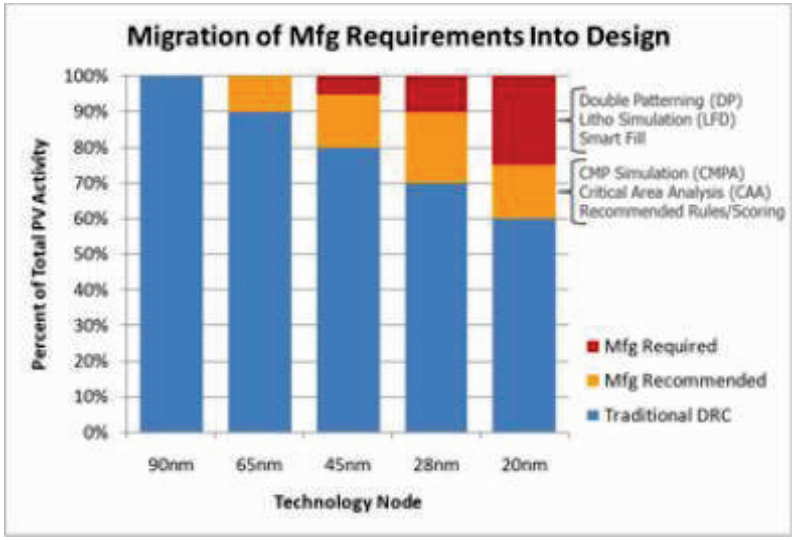
Typical per layer CPU Hours required to process full chip OPC by technology node.

J. Sturtevant. Proc. of SPIE Vol. 7639, 763902

Greater Dependence on Simulations

- With advanced 20nm and 14nm nodes – more lithography simulations required to assure new design is manufacturable.
- Ecosystems are formed – collaborative device manufacturing. Foundries, EDA, fabless customers





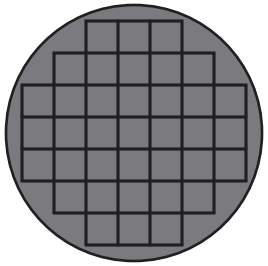
Practical Limits of Lithography

- Manufacturing processes all have variation
  - Should think of OPC as part of the mfg process
  - The magnitude of the variation
    - Tool and process control issues
  - The sensitivity to the variation
    - Design, RET and process issues
- Analysis of process variation key component of lithography development
  - Process Window analysis
  - MEF
  - Overlay
- These techniques are equally applicable to simulation and experiment

Process Window

- All variation combined into two values
  - Effective focus variation
  - Effective dose variation
- Sensitivity to process variation quantified in terms of:
  - Depth of focus
  - Exposure latitude
- “Elliptical Process Windows”
  - Can have direct correlation to sigma values of expected process variation

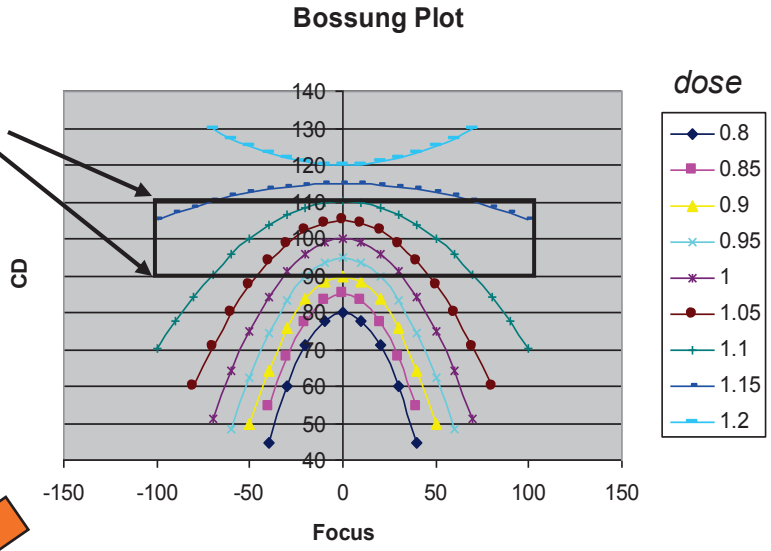
Defining Process Window

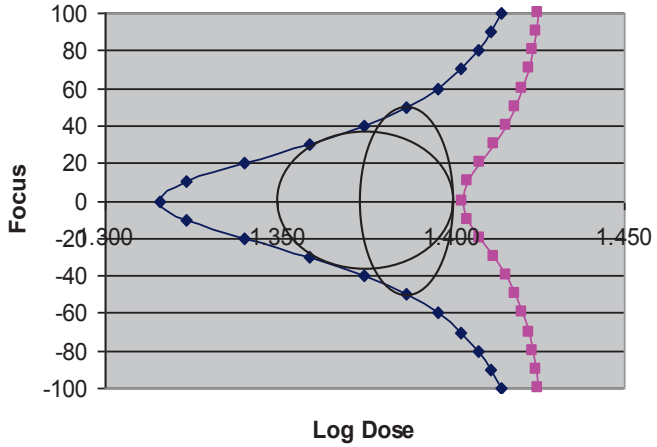


FEM Wafer

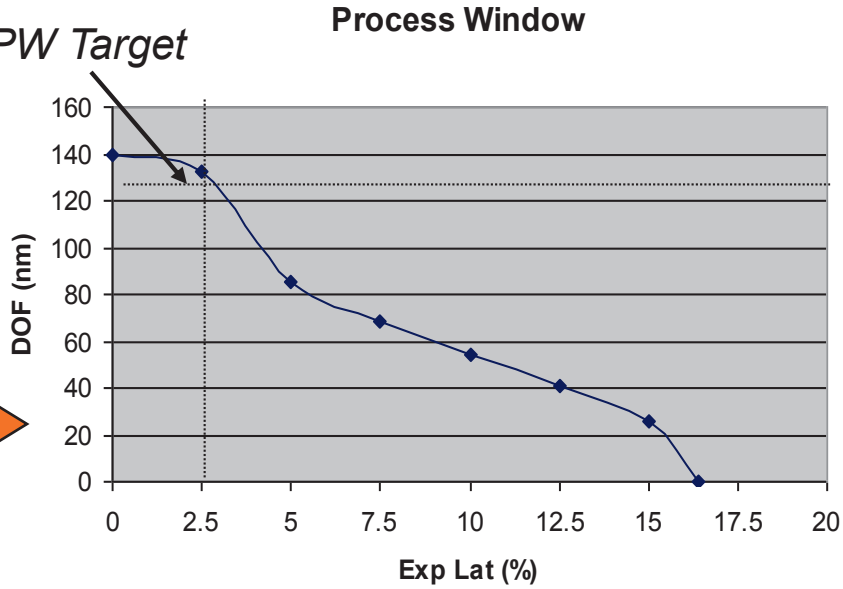
SEM Meas'ts

CD tolerances



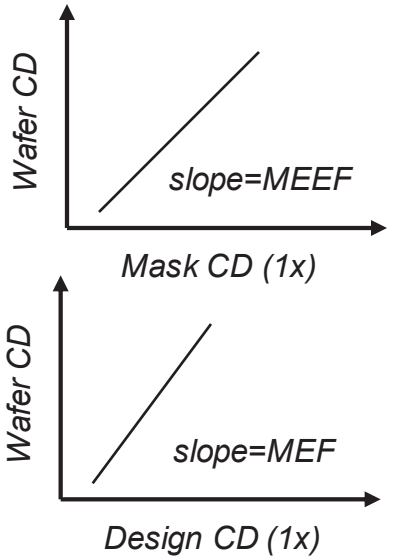


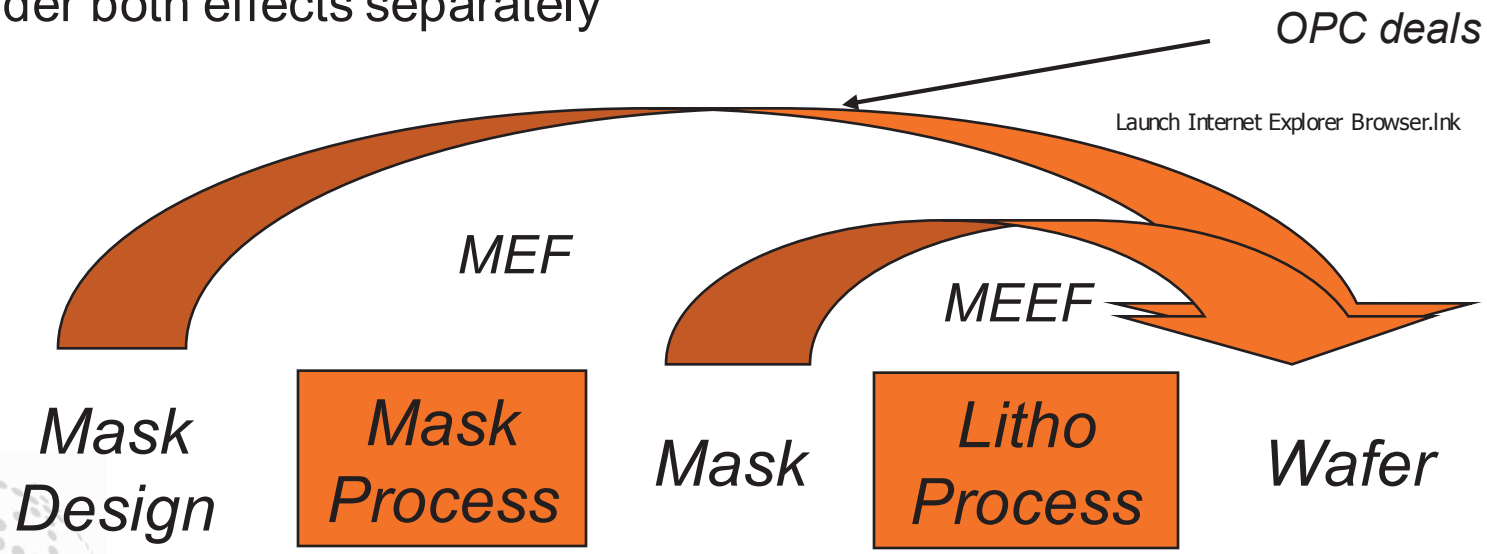
PW Target



MEF

- Mask Error Factor or Mask Error Enhancement Factor (MEEF)
- Describes sensitivity of wafer dimension to:
  - Mask dimension
  - Mask design dimension
- Two names, two distinct concepts, no consensus on which one is which
- In CL we often consider MEF, but with mask modeling we can consider both effects separately





Computational Lithography Process Optimization Tools

Design of Experiment

Test pattern generator

Exposure conditions

RET/OPC

Simulator

Lithography simulator

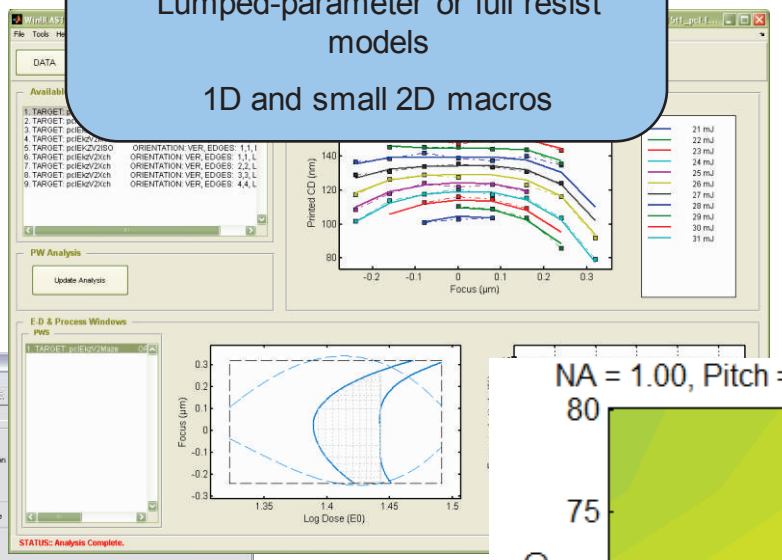
Lumped-parameter or full resist models

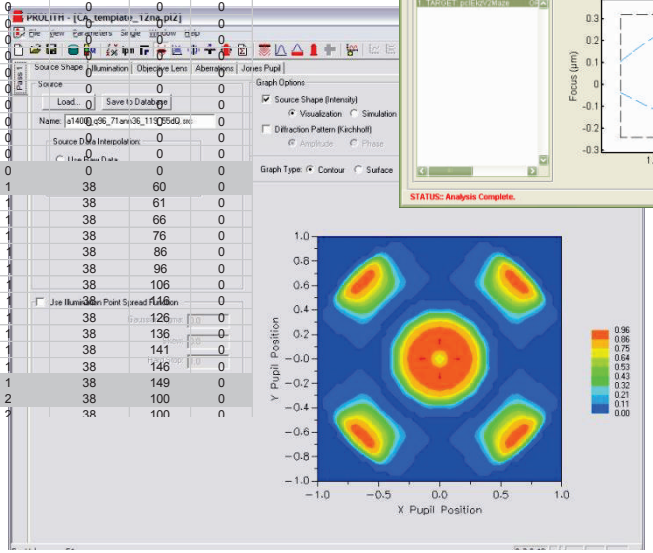
1D and small 2D macros

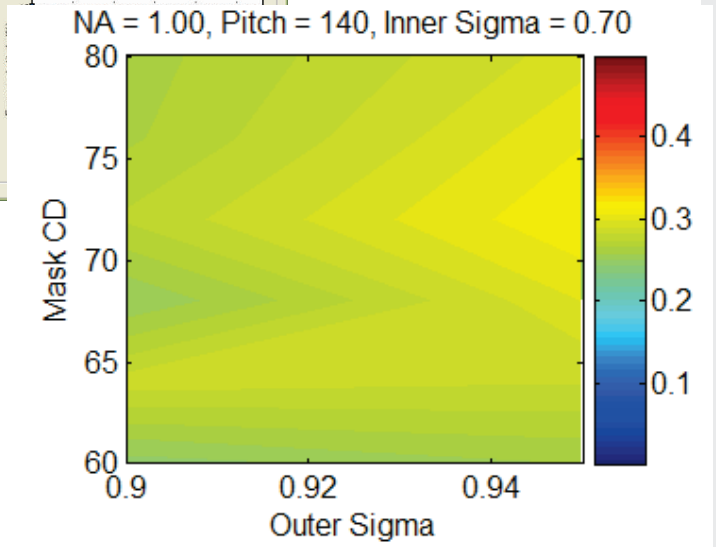
Analysis

Process window analysis

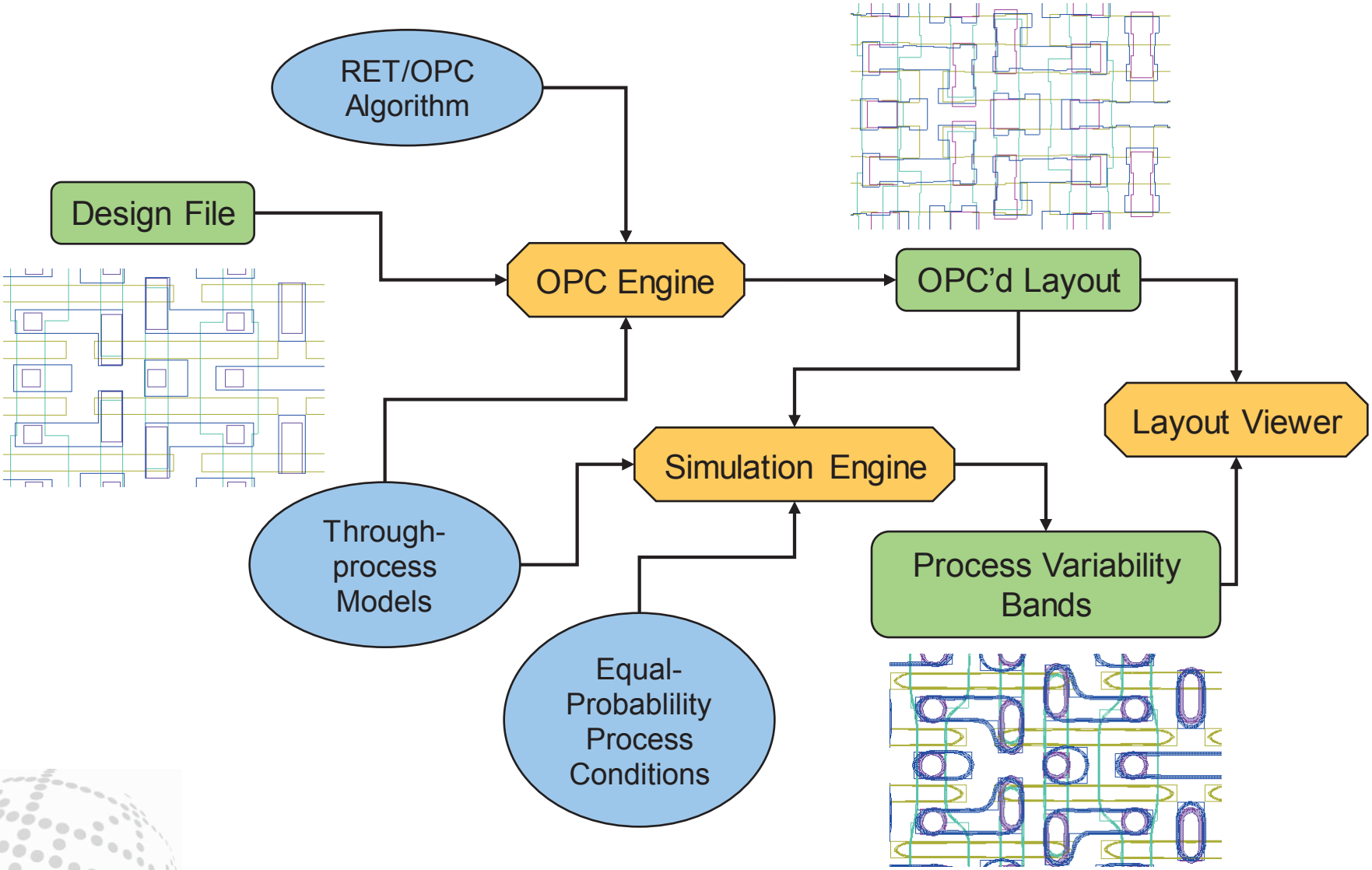
%Pitch	TargetCD	1.1NA/Q:0.65_0.85_45/3.8xE0	numAssists	assistSize	LOC_1	LOC_2
130	70	77.4	0	0	0	0
135	70	78.1	0	0	0	0
140	70	78.6	0	0	0	0
145	70	79.3	0	0	0	0
150	70	79.7	0	0	0	0
155	70	79.8	0	0	0	0
160	70	80.0	0	0	0	0
180	70	81.9	0	0	0	0
190	70	84.6	0	0	0	0
200	70	87.7	0	0	0	0
210	70	90.5	0	0	0	0
220	70	92.9	0	0	0	0
228	70	94.2	0	0	0	0
228	70	89.4	1	38	60	0
230	70	89.5	1	38	61	0
240	70	89.7	1	38	66	0
260	70	90.1	1	38	76	0
280	70	89.8	1	38	86	0
300	70	89.7	1	38	96	0
320	70	89.7	1	38	106	0
340	70	90.5	1	38	116	0
360	70	92.2	1	38	126	0
380	70	95.3	1	38	136	0
390	70	96.7	1	38	141	0
400	70	98.2	1	38	146	0
406	70	98.8	1	38	149	0
406	70	90.0	2	38	100	0







Tools - Lithography Manufacturability Assessor



ORC- Built-in detectors

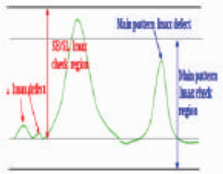
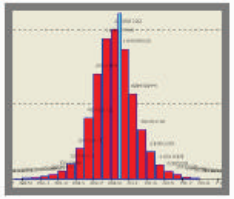


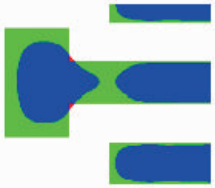
Image quality: ILS, Imin, Imax



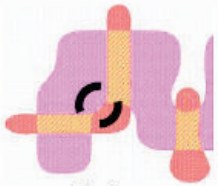
Full chip CDU optimization

Edge Placement error

All angle bridging

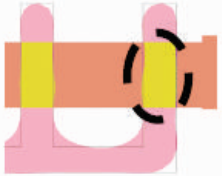


All angle necking

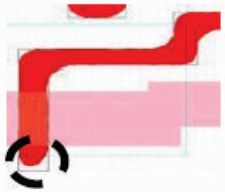


Poly-active short

Thru-PW C2C / MEEF



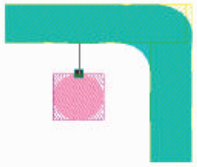
CDU / CDV



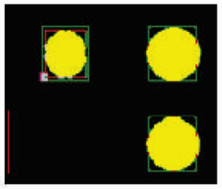
Line-end / end-cap

Extra printing feature: SRAF, side lobe

Contact enclosure



Contact exclosure

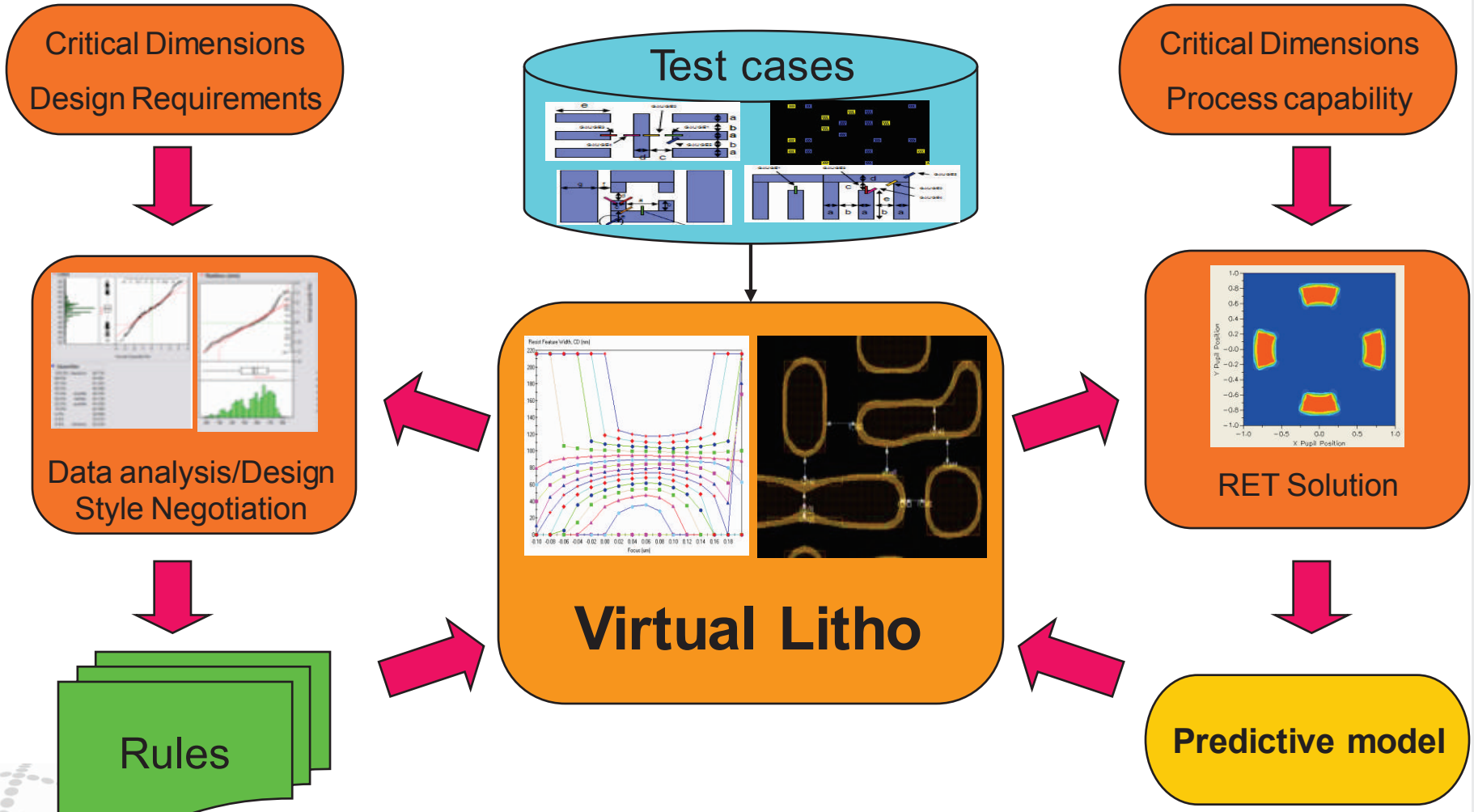


Contact area

Outline

- RET Selection
  - Evaluation of various RET per level
  - Optimization of the RET/litho/dataprep process in simulation/experiment
  - Must be done in conjunction with design rule specification
- RET Process Development
  - Film stack optimization
  - Resist and etch process optimization
  - Integration
- RET Application Development
  - Creation of application code for dataprep
  - Generally includes decomposition, SRAF placement and MBOPC
- Examples

Interaction of RET Selection and Design Rule Creation



RET Selection - Example

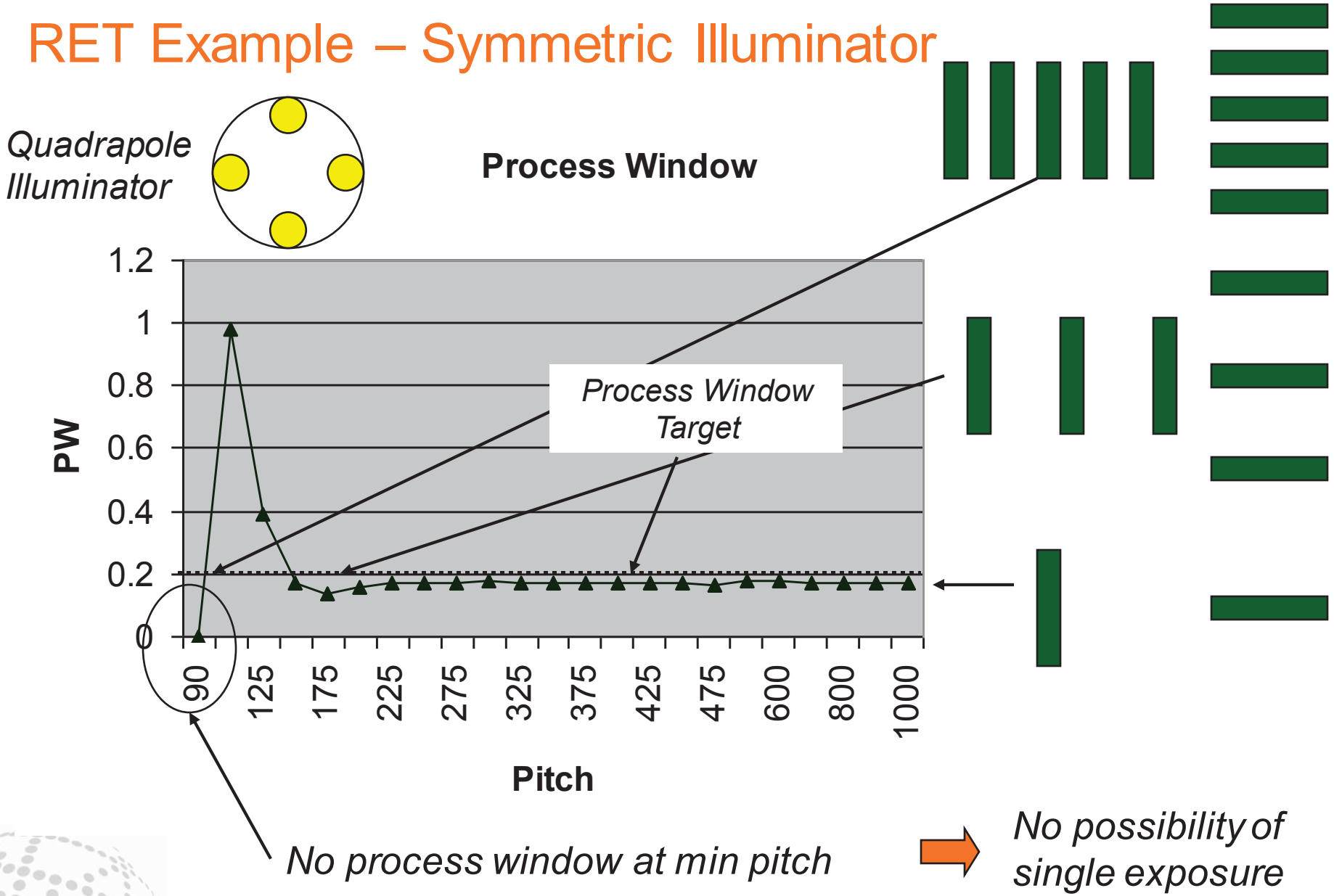
- Say you want to print a 90 nm pitch metal level using a 193nm, 1.2NA exposure tool

- Where do we start?
  - k1 = NA * half-pitch / lambda = 0.28
  - Strong off-axis illumination or double exposure required

- What are process window/MEF requirements?
  - Determine expected focus, dose and mask variations
  - Set targets accordingly

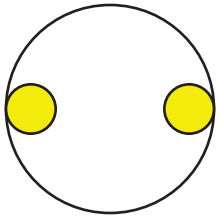
- What are acceptable design restrictions?
  - Minimum line only required for pitch < 180 nm
  - Minimum space only required for pitch < 180 nm

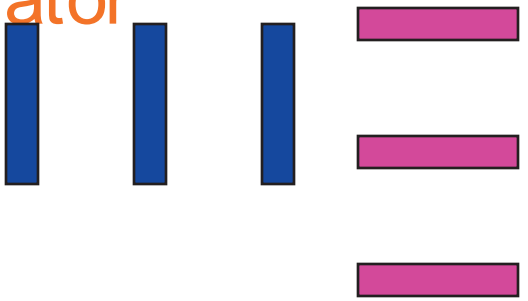
RET Example – Symmetric Illuminator



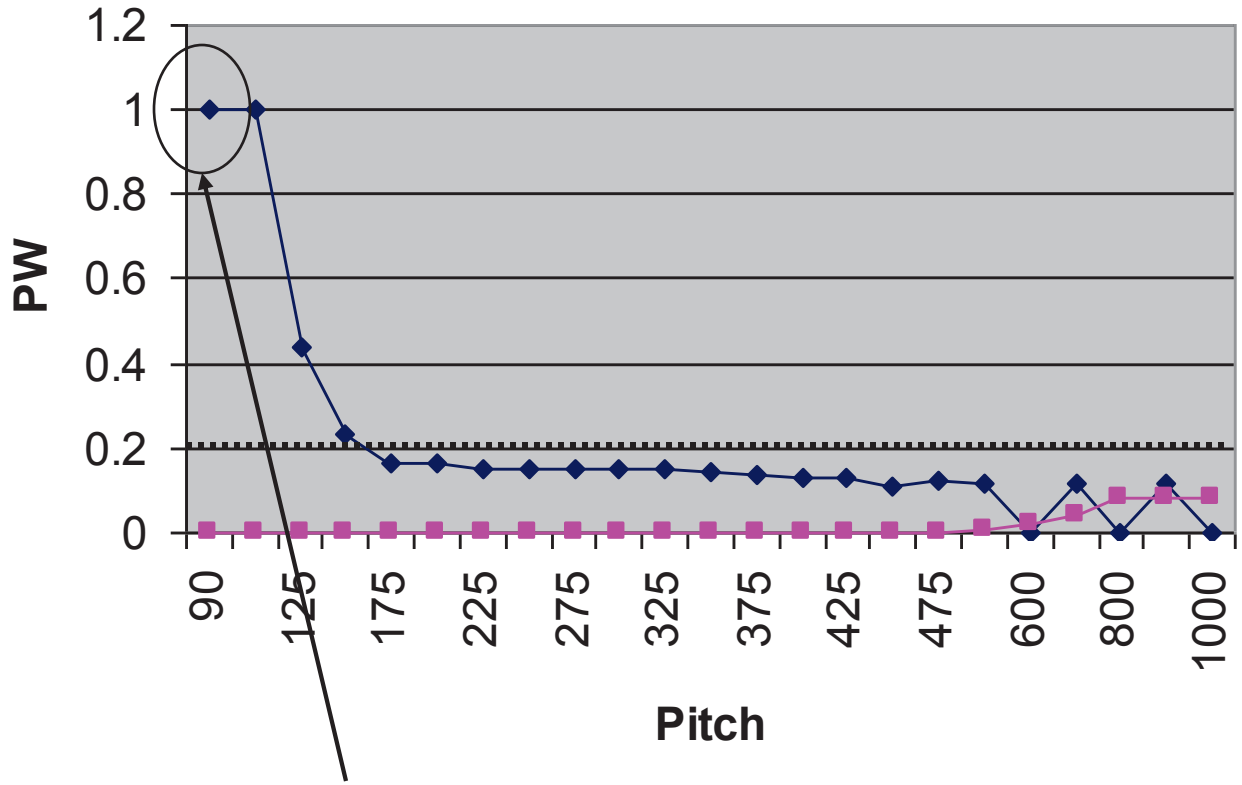
RET Example – Assymmetric Illuminator

Dipole Illuminator



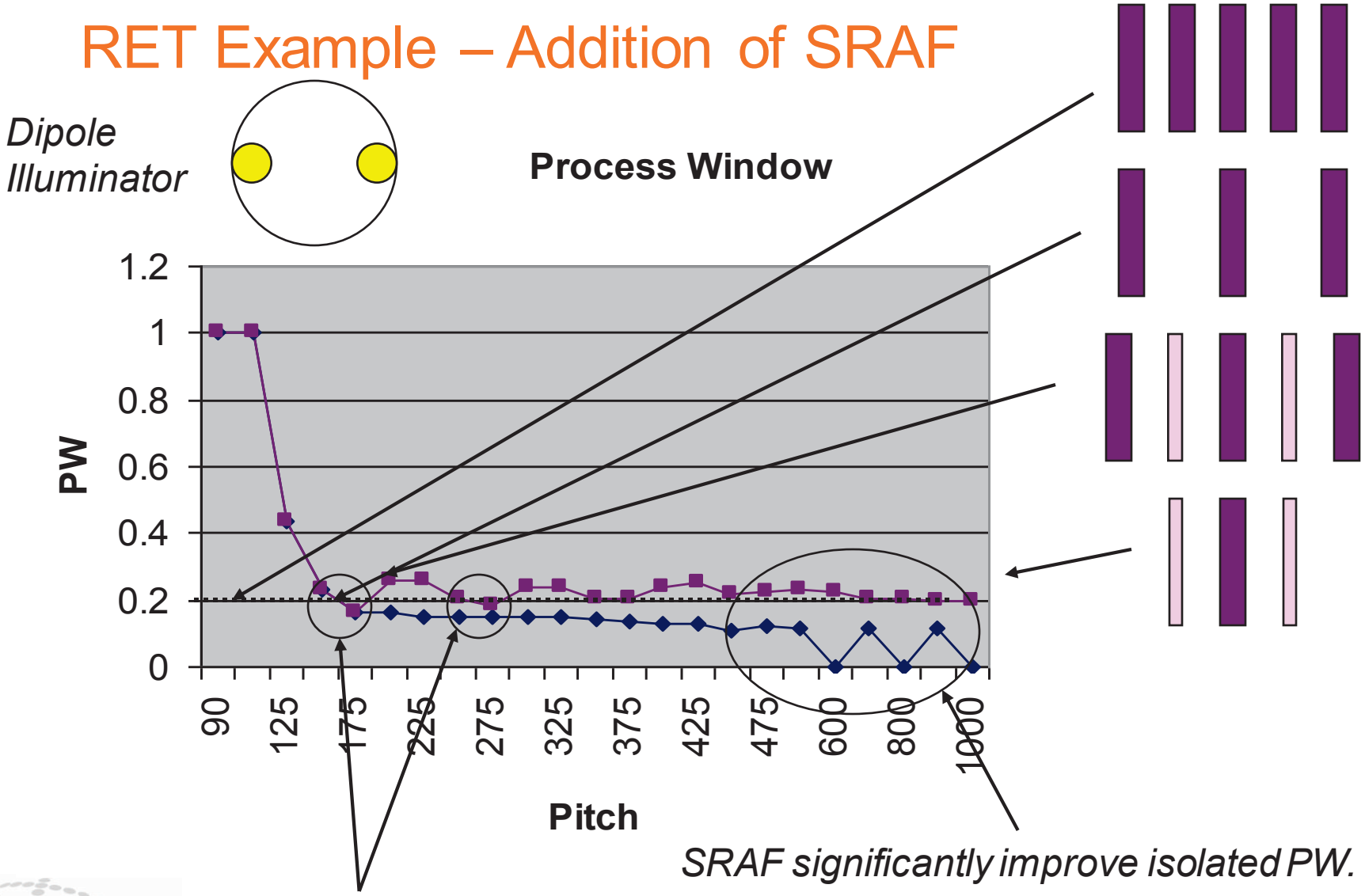


Process Window

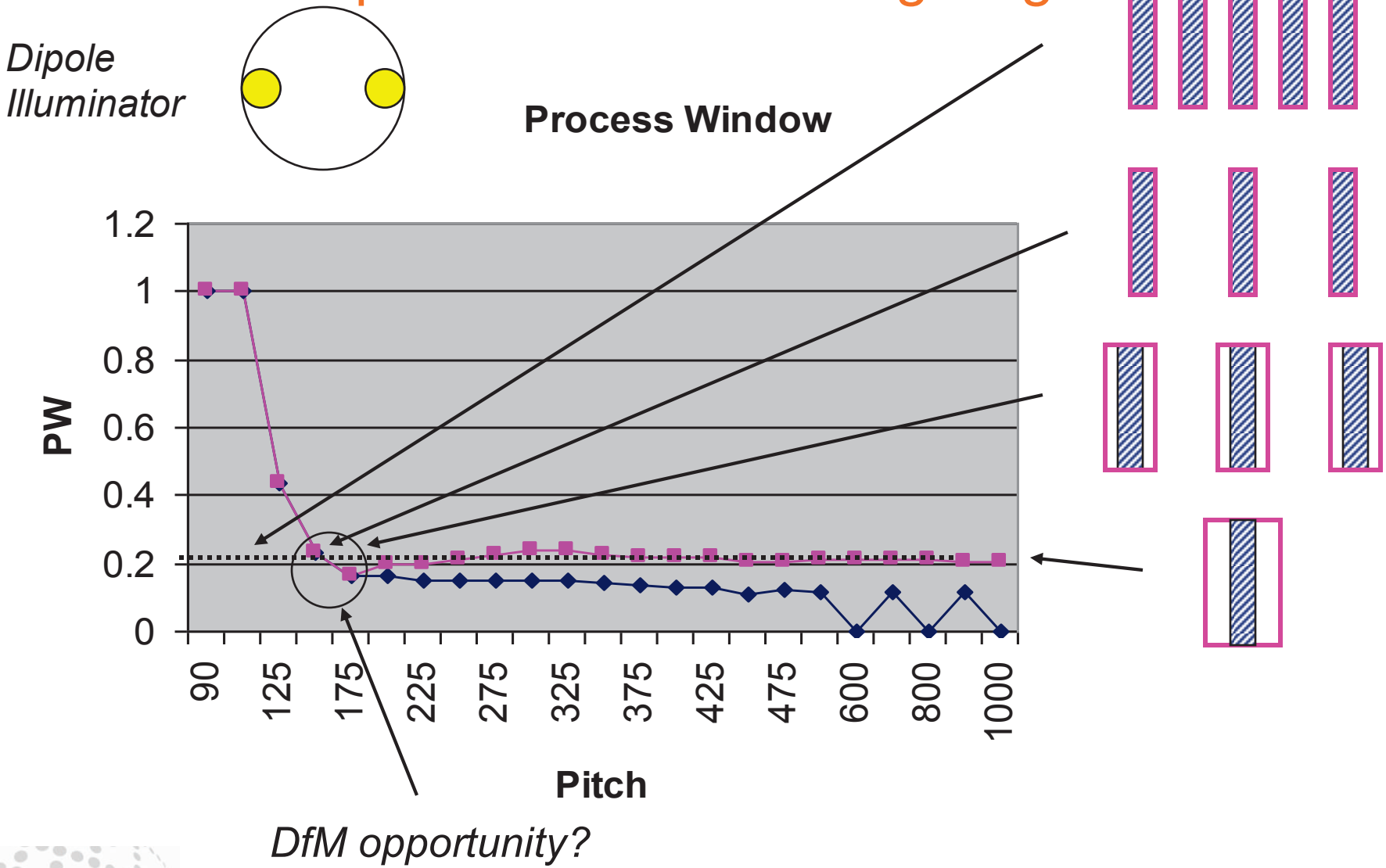


Adequate process window at min pitch – but highly orientation dependent.

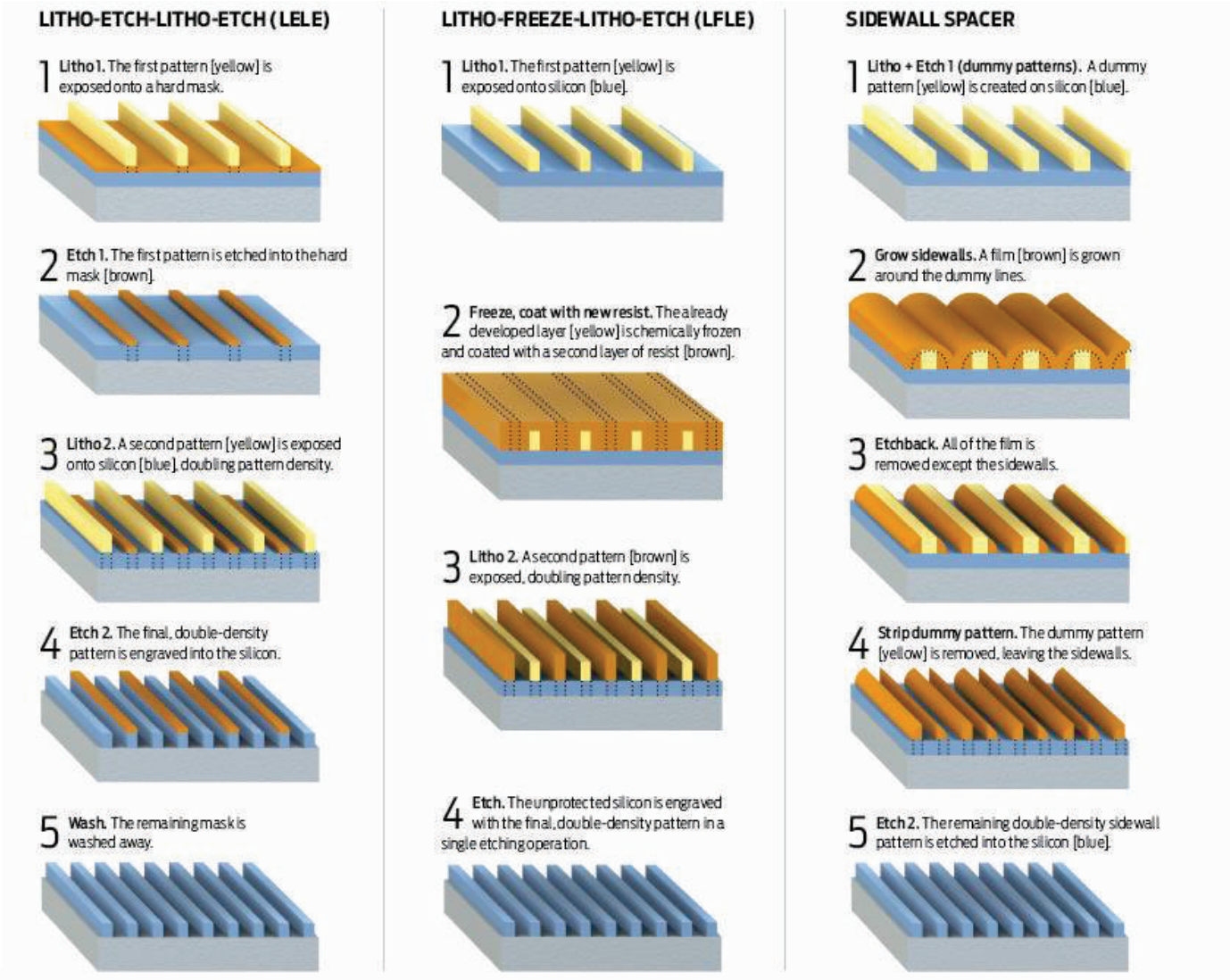
RET Example – Addition of SRAF



RET Example – Selective Retargeting



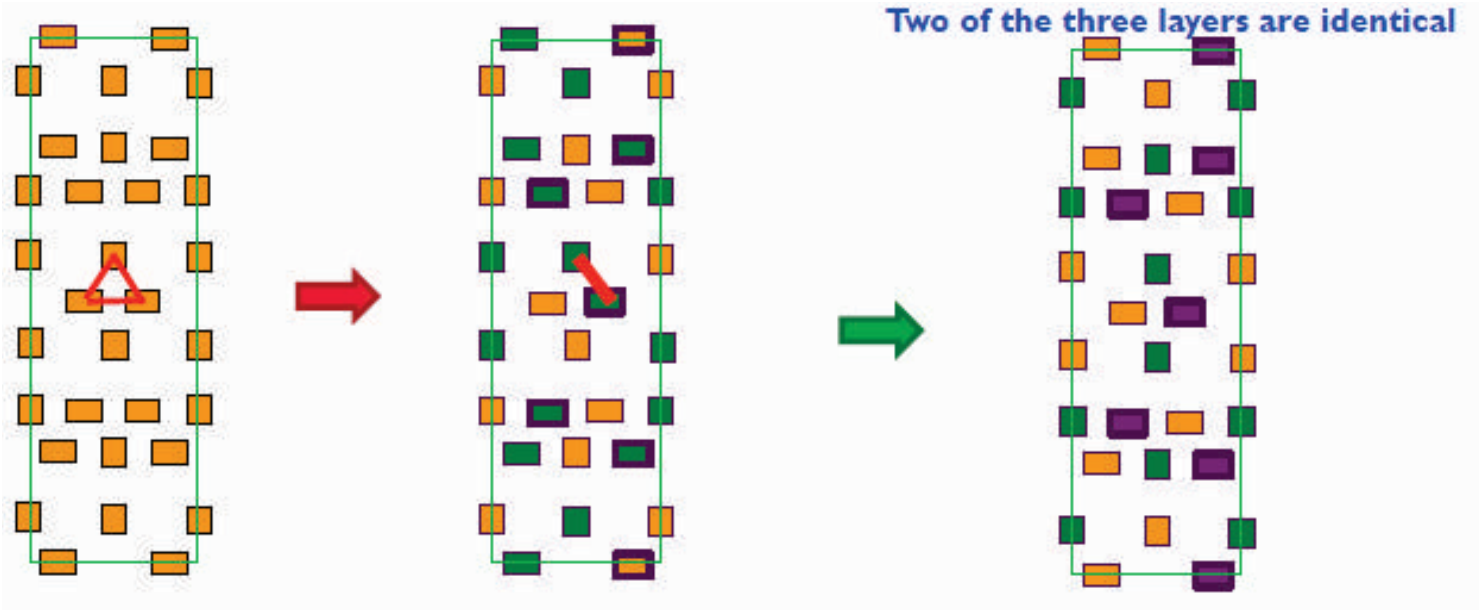
Double Patterning Lithography



Common set of problems for double patterning

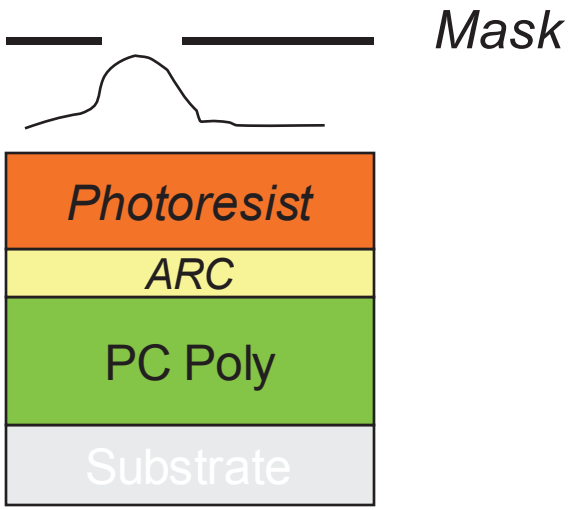
Triple Patterning

Single Patterning | Double Patterning | Triple Patterning

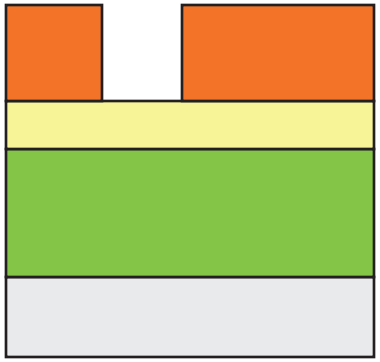


Critical triangle | Critical doublet | Proximity conflict solved

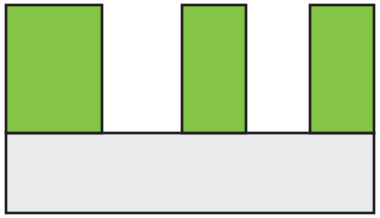
Single Exposure Process



1. Coat resist, expose mask 1

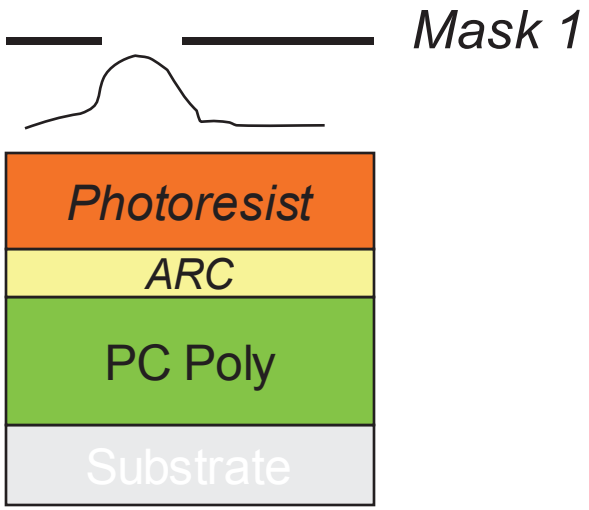


2. Develop resist

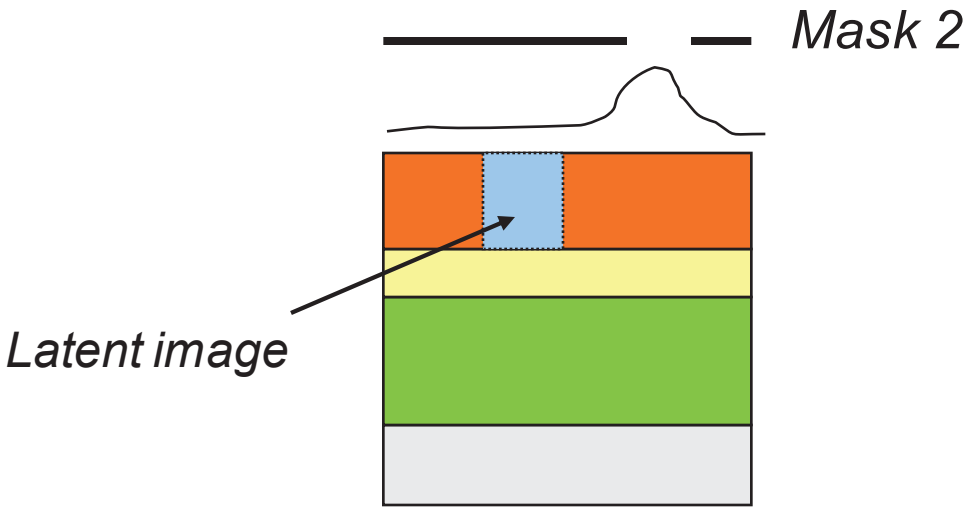


3. Transfer into Poly

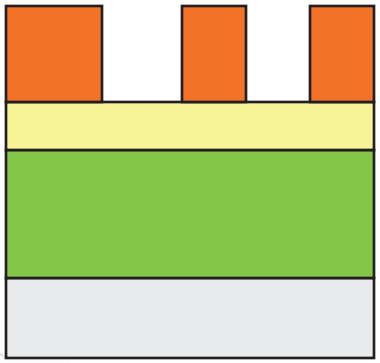
Double Exposure Process



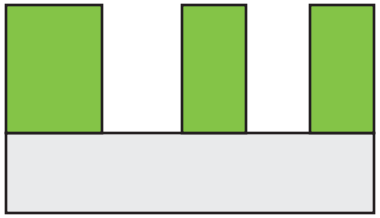
1. Coat resist, expose mask 1



2. Expose mask 2



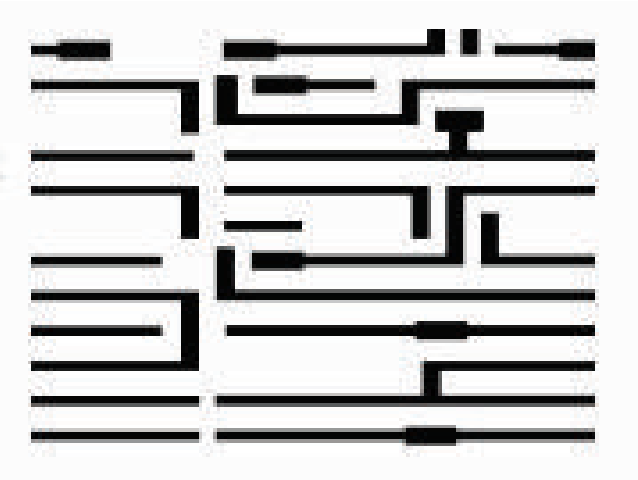
3. Develop resist

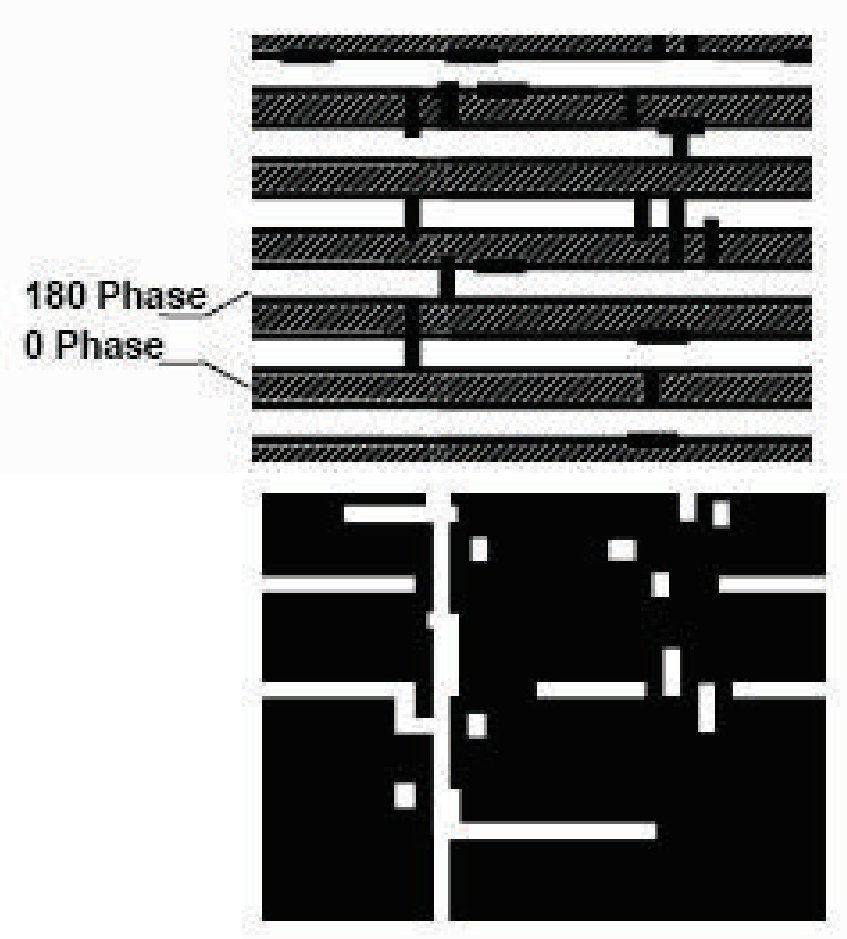


4. Transfer into Poly

Double Exposure – Alternating Phase Shift

Poly input layer



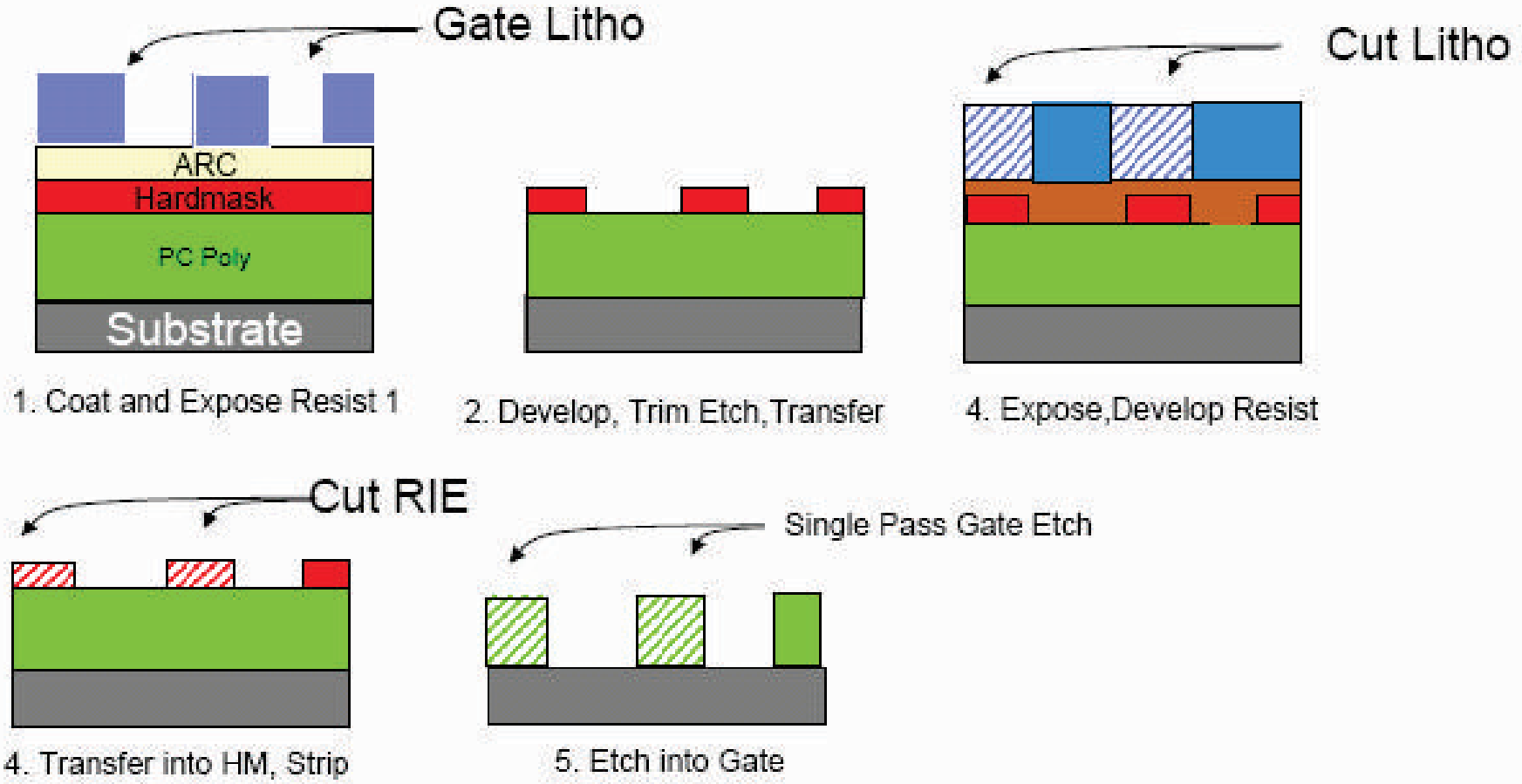


Phase mask

Block mask

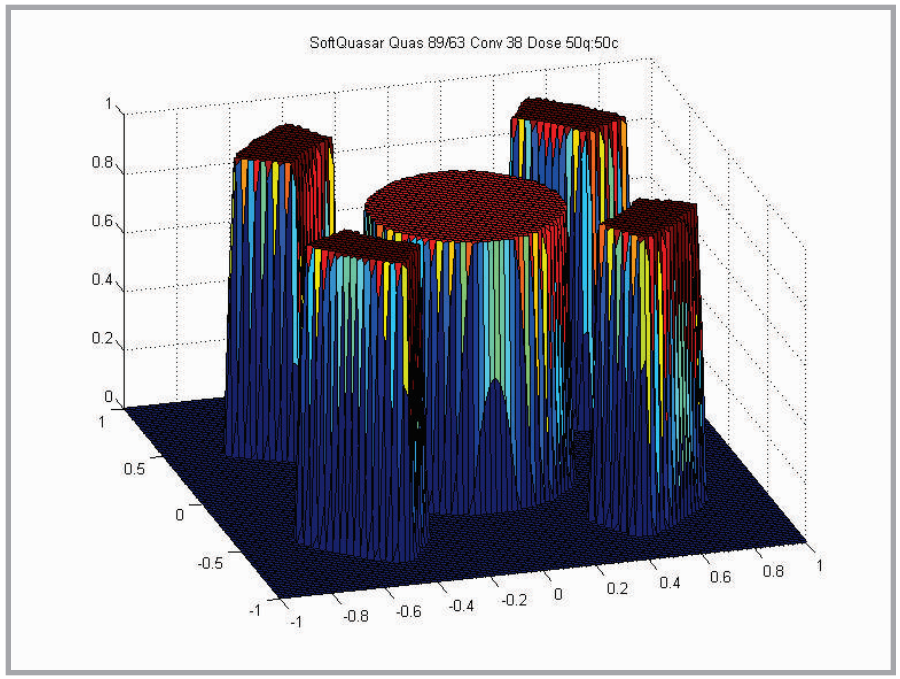
High-performance circuit design for the RET-enabled 65-nm technology node
Lars W. Liebmann, Arnold E. Barish, Zachary Baum, Henry A. Bonges, Scott J. Bukofsky, Carlos A. Fonseca, Scott D. Halle, Gregory A. Northrop, Steven L. Runyon, and Leon Sigal
Proc. SPIE **5379**, 20 (2004)

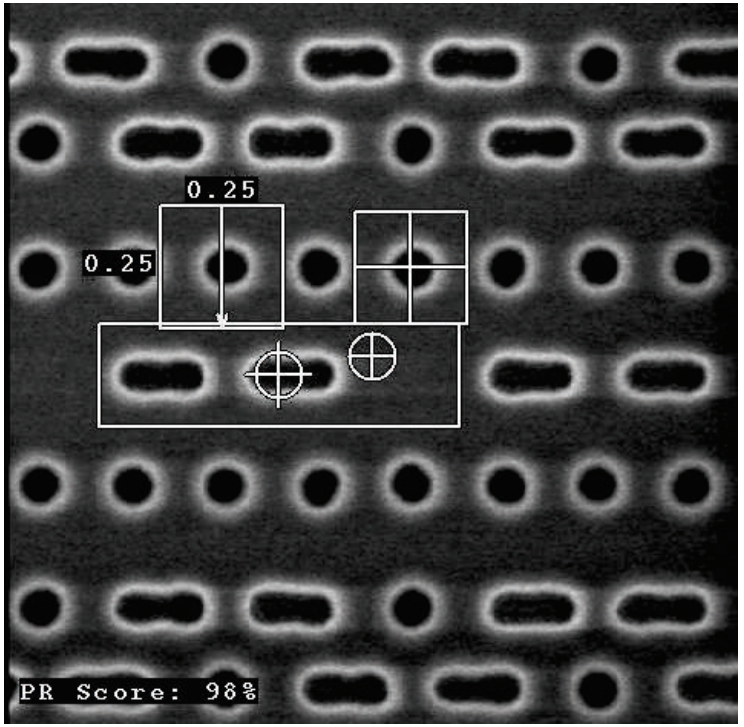
Double Exposure Double Etch (DE^2) Process



Complex and expensive process!

Optimized Illumination

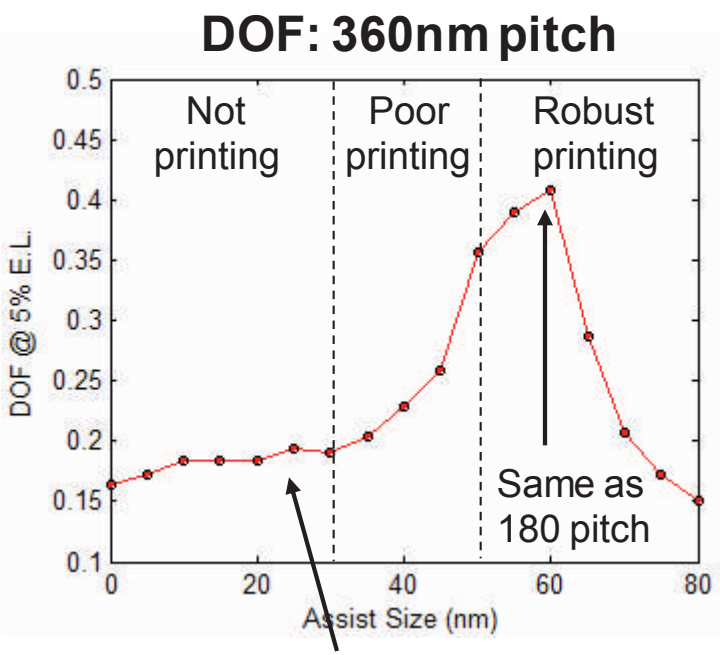




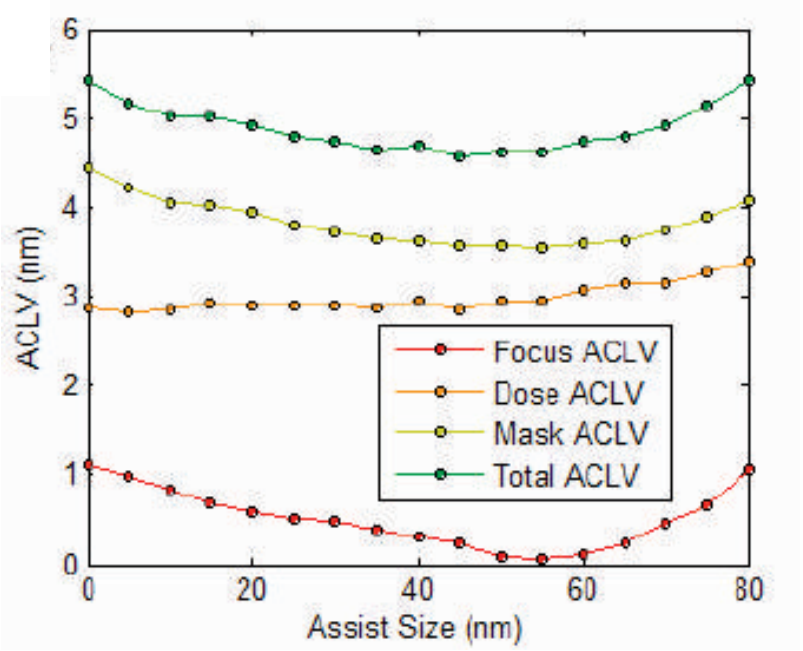
- Illumination optimized to improve through-pitch process window and improve SRAM printing.

Lithography process optimization using linear superposition of commonly available illumination modes
Michael M. Crouse, Yasri Yudhistira, Min Ho Lee, and Hope Matis
Proc. SPIE **6154**, 61541Q (2006)

Assist Features - RET Selection



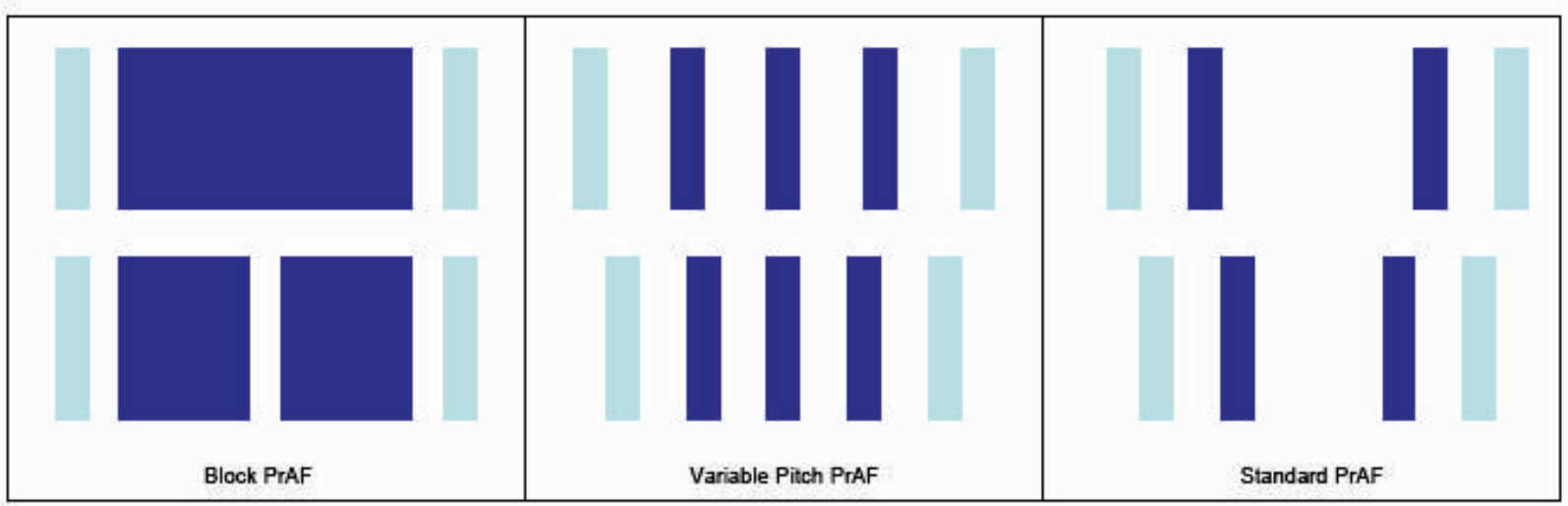
Best achievable DOF with SRAF

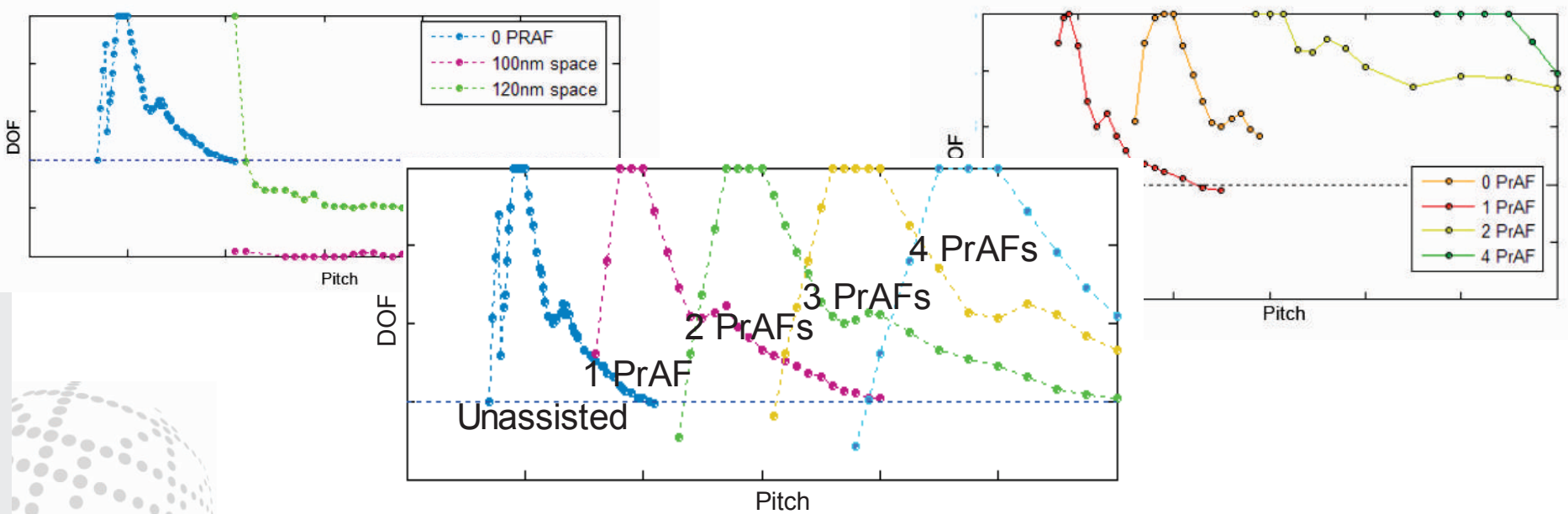


Across-chip linewidth variation (ACLV) for specific focus, dose and mask variations.

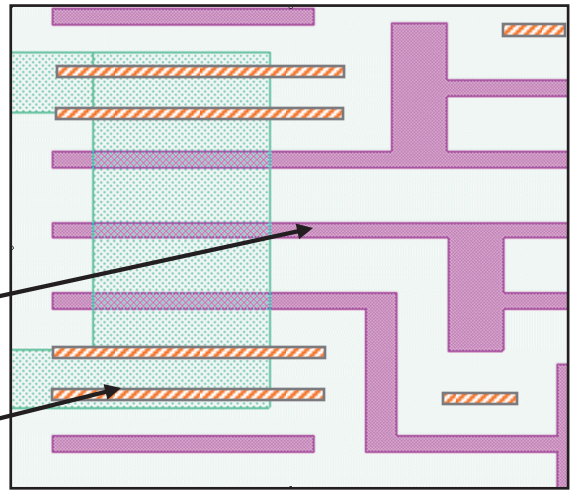
J. Meiring et al. **ACLV driven double-patterning decomposition with extensively added printing assist features (PrAFs)** Proc. SPIE **6520**, 65201U (2007)

RET Selection - PrAF Type

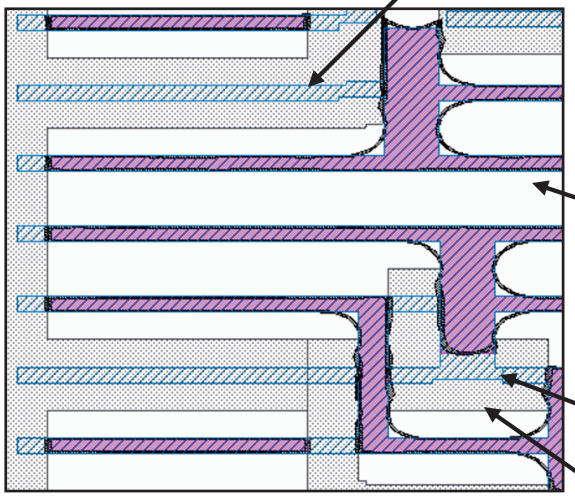


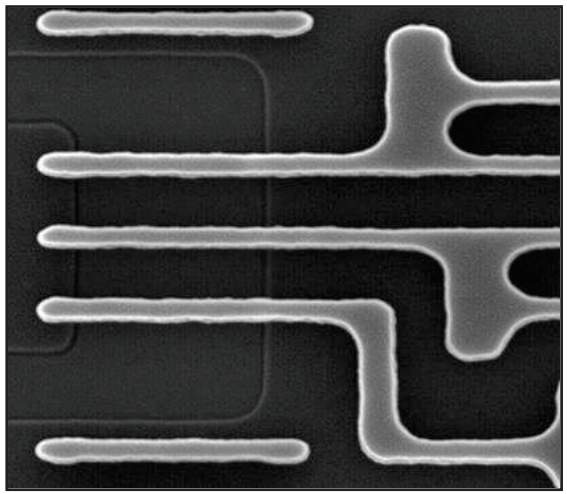


Results - SRAF vs PRAF/Cut Mask

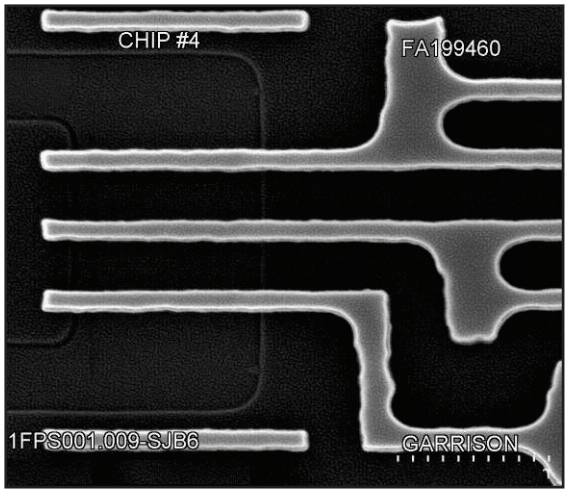


Designed pattern magenta, SRAF cross-hatched





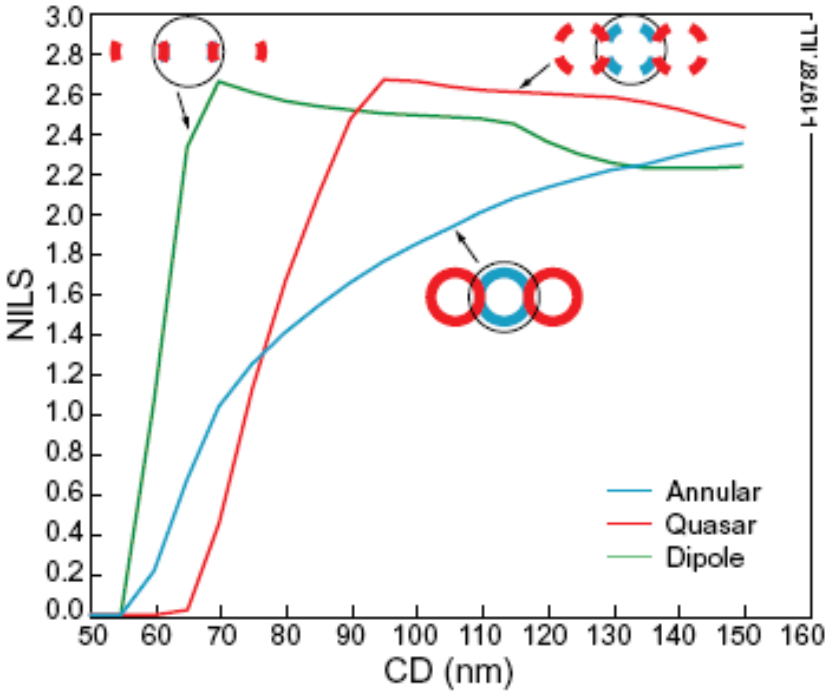
Single Exposure

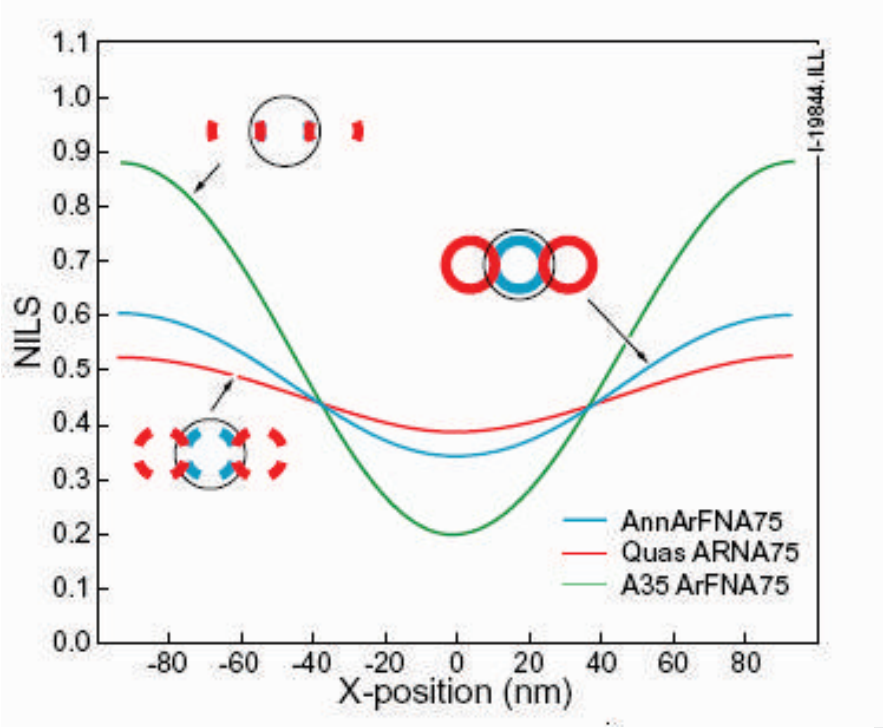


DE² Process

"Paving the way to a full-chip gate-level double-patterning application," H. Haffner, Z. Baum, S. Halle and J.Meiring

Dipole Lithography – RET Selection





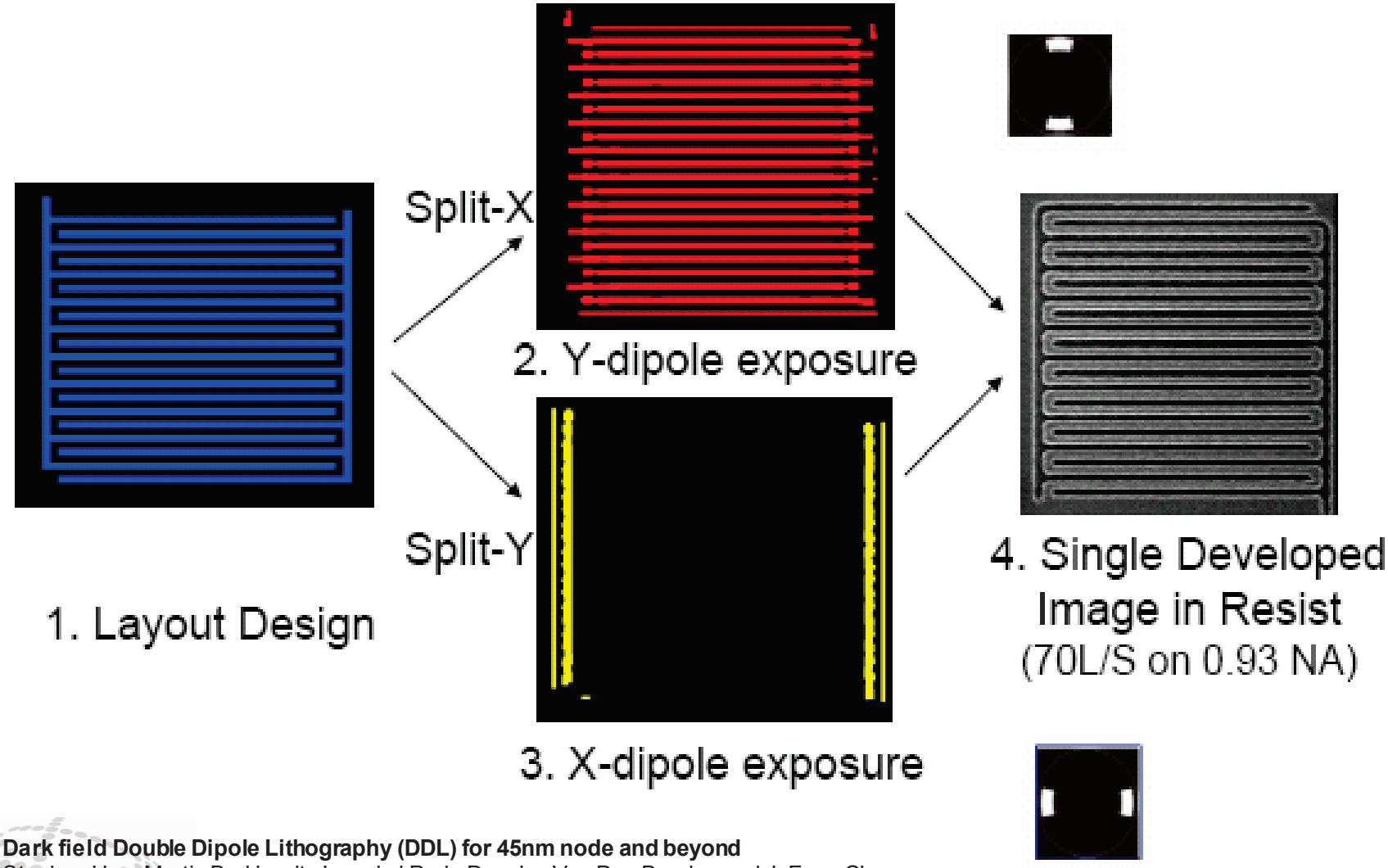
Dipole shows improved contrast for small CD's.

70nm line on 170nm pitch

193nm, 0.75NA

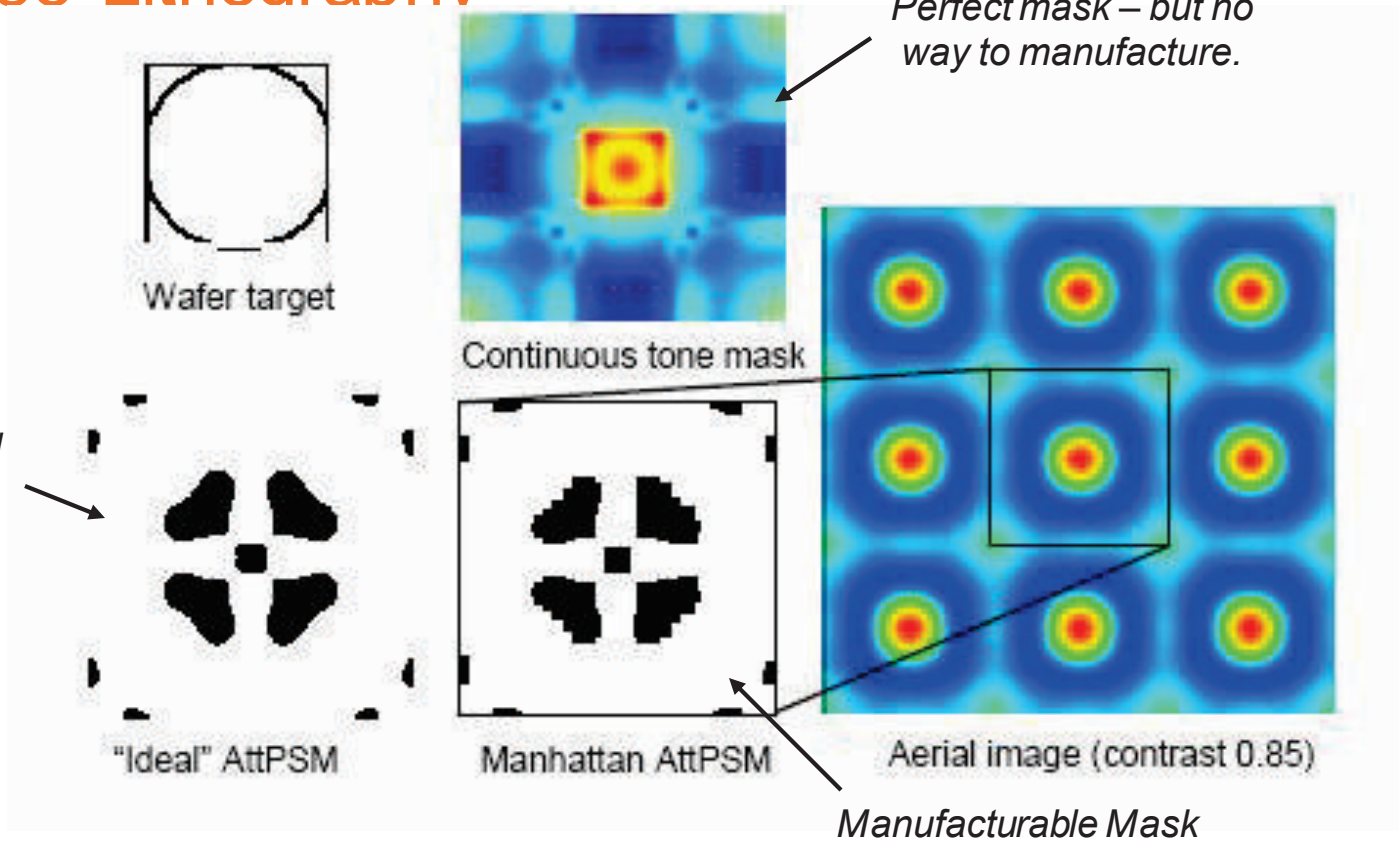
Dipole decomposition mask design for full-chip implementation at 100-nm technology node and beyond
Stephen Hsu, Noel P. Corcoran, Mark Eurlings, William T. Knose, Thomas L. Laidig, Kurt E. Wampler, Sabita Roy, Xuelong Shi, Chungwei Michael Hsu, J. Fung Chen, Jo Finders, Robert J. Socha, and Mircea V. Dusa
Proc. SPIE **4691**, 476 (2002)

Double Dipole Lithography



Dark field Double Dipole Lithography (DDL) for 45nm node and beyond
Stephen Hsu, Martin Burkhardt, Jungchul Park, Douglas Van Den Broeke, and J. Fung Chen
Proc. SPIE **6283**, 62830U (2006)

Inverse Lithography



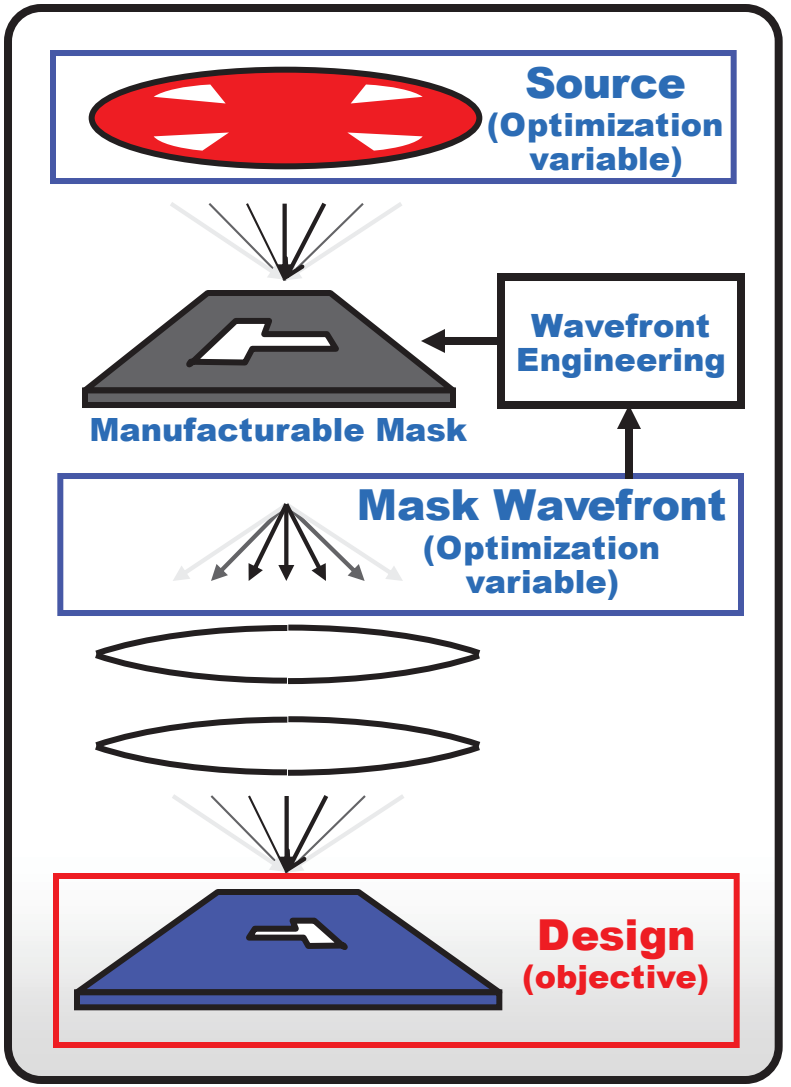
Optimum mask shapes determined to print final wafer target. These mask shapes do not need to look anything like final target and can include many "unattached" features. Concept of "assist features" is automatically included.

Interesting study of benefits/ drawbacks to mask industry. ⇨

Inverse Lithography Technology (ILT): what is the impact to the photomask industry?
Linyong Pang, Yong Liu, and Dan Abrams
Proc. SPIE **6283**, 62830X (2006)

Global Source-Mask Optimization

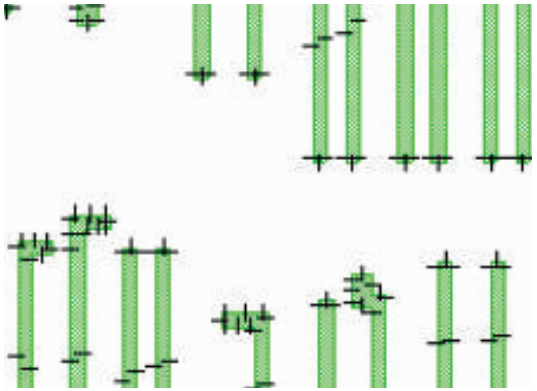
- Algorithm engages true degrees of freedom in the imaging process
- Global algorithms can often yield fundamentally better solutions
- Mathematically derived solutions need not look like starting design
- Distinctly different solutions from conventional RET methods
- Can be coupled with Deep Computing for large areas



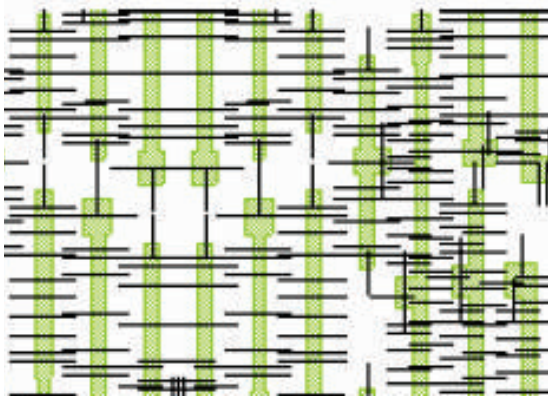
Dense OPC

Grid-based simulation more efficient with increasing layout density

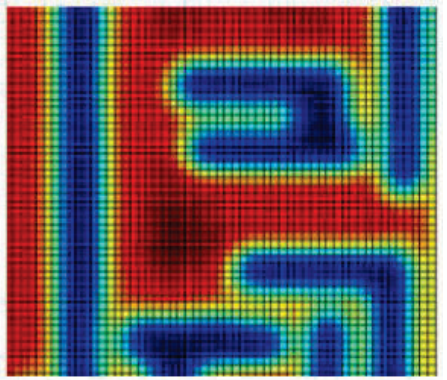
180nm sparse simulation



45nm sparse simulation



45nm dense simulation



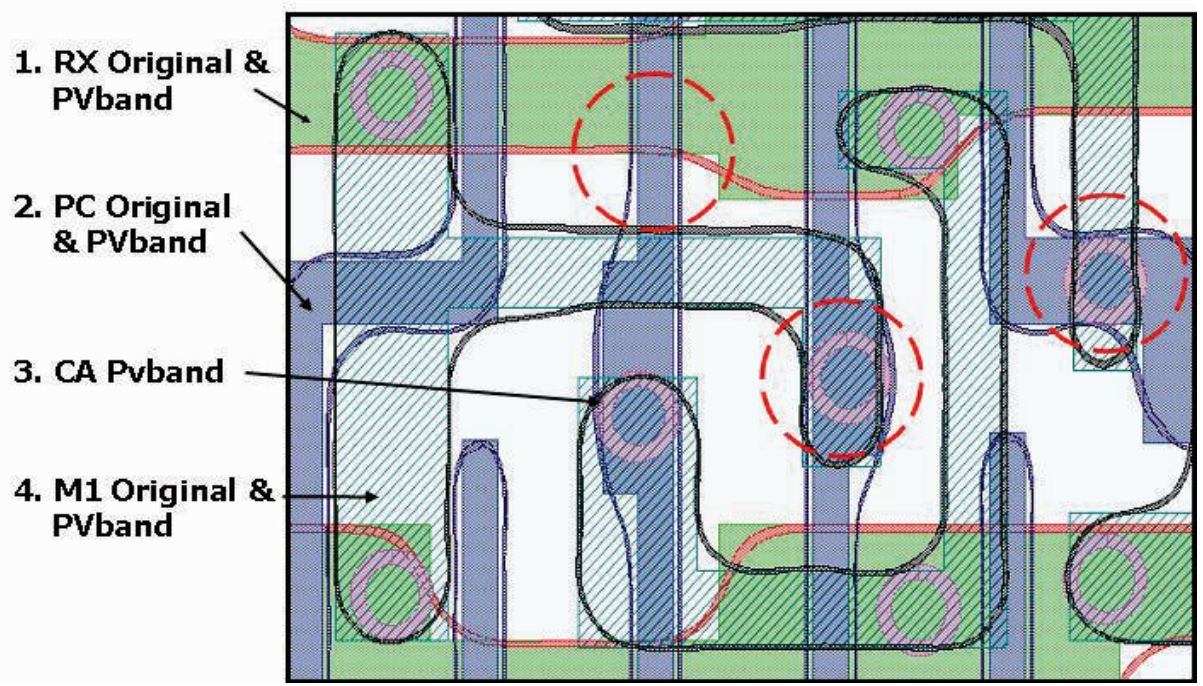
Dense has additional advantages:

- Algorithms that can be run on hardware accelerators
- Automated fragmentation of layout (post-simulation)
- Integration with pixel-based ("inverse lithography") algorithms
- Improved checking algorithms for verification

Dense OPC and verification for 45nm
Nicolas Cobb and Dragos Dudau
Proc. SPIE **6154**, 61540I (2006)

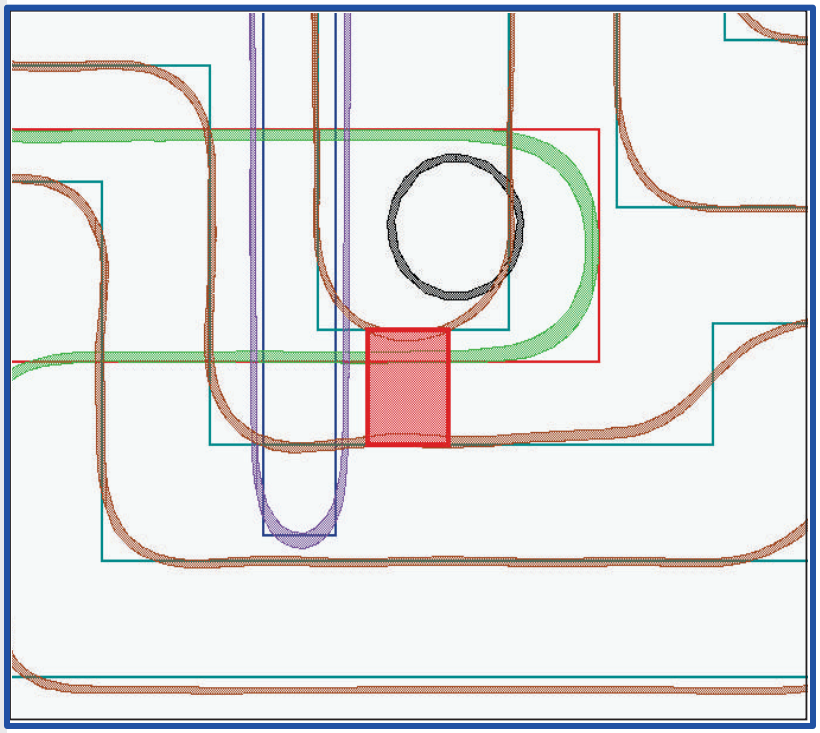
Litho-aware Layout, Opportunity

- In litho-aware layout, designers complement traditional design rules with direct litho modeling to achieve physical and parametric yield targets for aggressive layouts in resolution challenged technology nodes. Layout, process variability bands, opportunities for enhancement:



Slide courtesy of Lars Liebmann

Litho-aware Layout, Benefits/Challenges



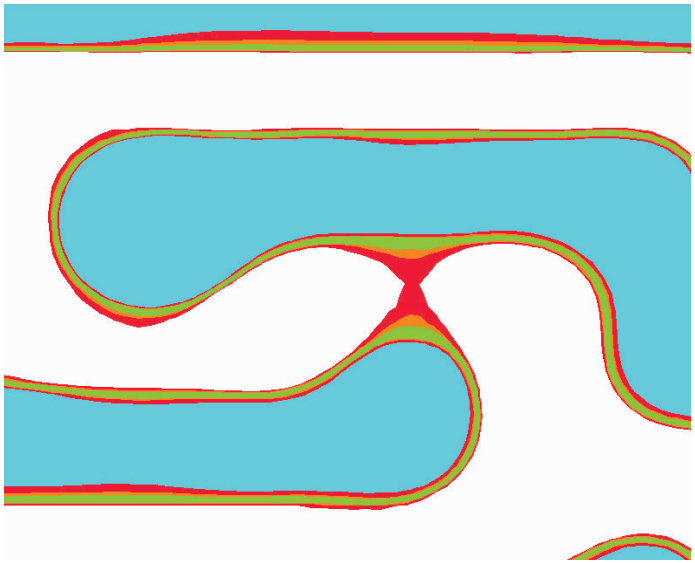
Benefits:

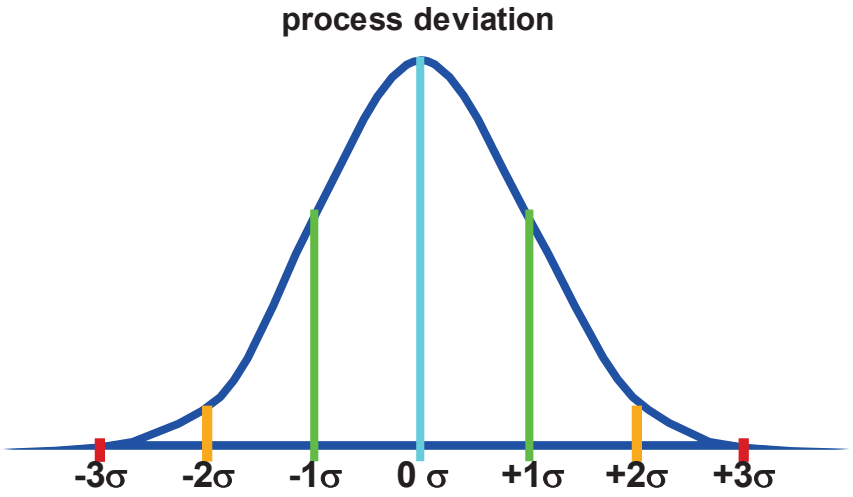
- **Catch RET or OPC problems early and outside the critical path**
- **Alert designers of unmanufacturable or extremely variability-sensitive layouts**
- **Help designers visualize manufacturability concerns to drive optimized tradeoffs**

Integration Challenges:

- **Accuracy vs. runtime**
- **Process stability over time**
- **Fab portability of the optimized layout**
- **Accurate identification of 'designer-actionable' hotspots**

Litho-aware Layout, Litho-variation to Yield correlation





statistical analysis of layout-process interactions can be correlated to process-limited yield

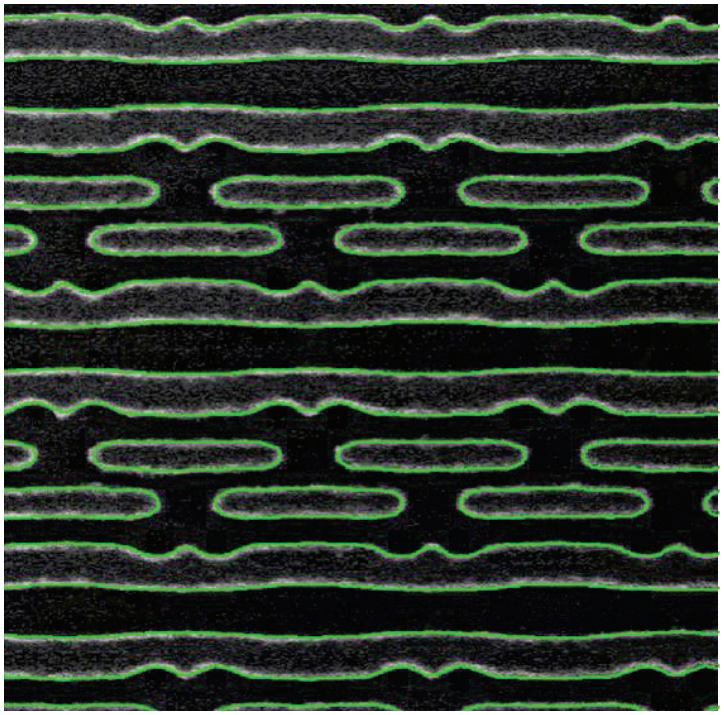
Reducing DfM to practice: the lithography manufacturability assessor
Lars Liebmann, Scott Mansfield, Geng Han, James Culp, Jason Hibbeler, and Roger Tsai
Proc. SPIE **6156**, 61560K (2006)

Predictive Modeling: Time to Market

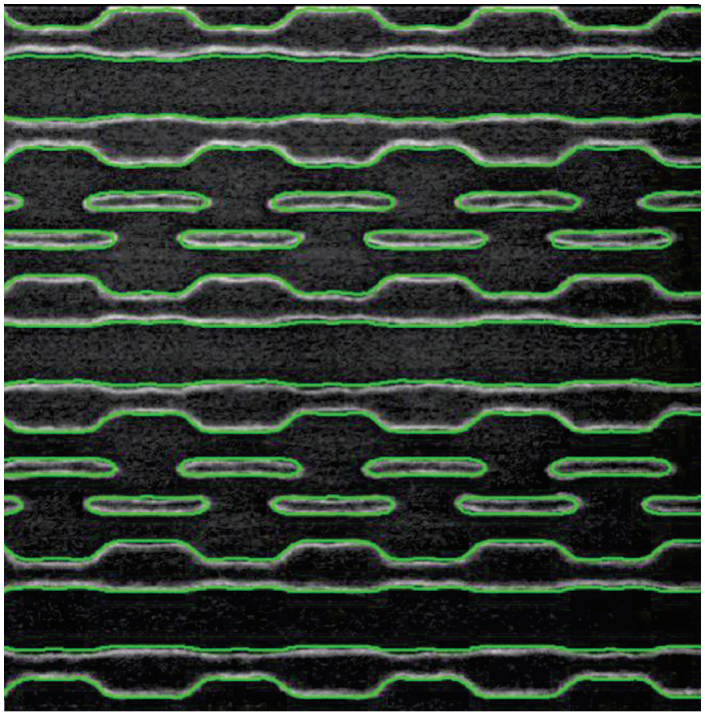
- Predictive modeling affords first time right

SRAM Active Area

45 nm cell: sub-0.250 μm^2



32 nm cell: sub-0.200 μm^2



1st Wafer Results

Predictive Modeling & Deep Computing

Scientific Process Modeling

- Rigorous but slow
- Limited to small areas
  - Understand physical effects
  - Calibrate approximate models

- Computationally intensive
  - Large Linux Clusters
  - BlueGene

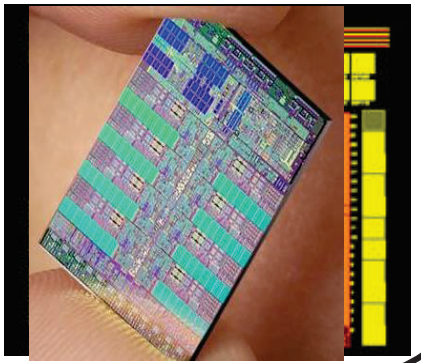
m
@ wafer

Resource-Efficient Modeling

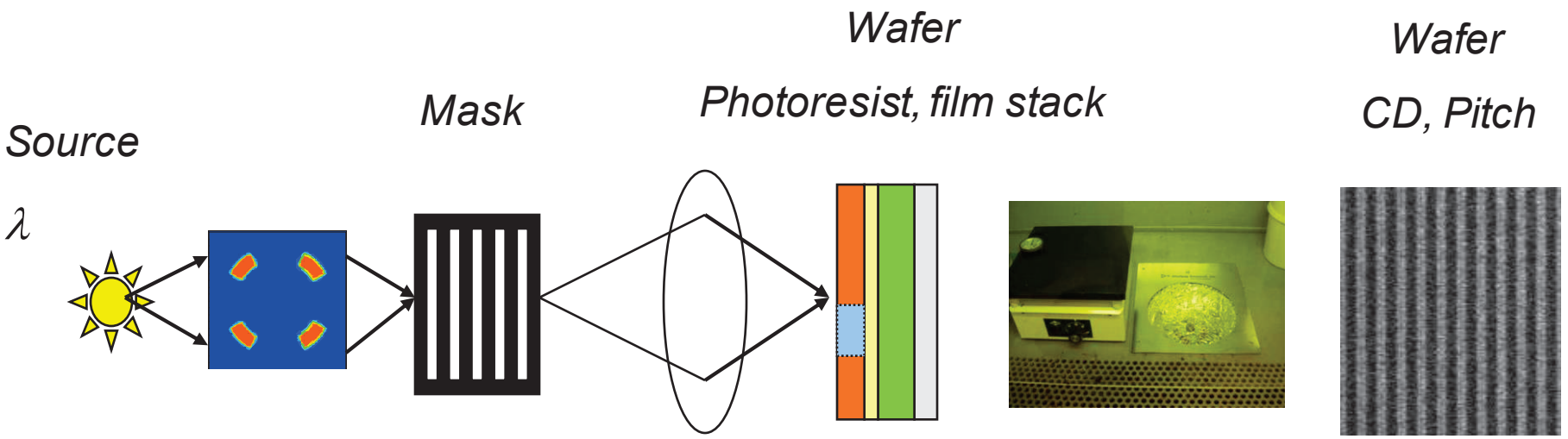
- Approximate & fast
- Can do large areas (full chip)
  - OPC & Verification

- Also computationally intensive
  - Blades with Acceleration
  - 100's of CPUs

26 mm
Cell BE
@ wafer



Elements of Predictive Modeling



Illumination Optics

Mask

EMF

Imaging Optics

Photoresist Exposure and Develop

Etch

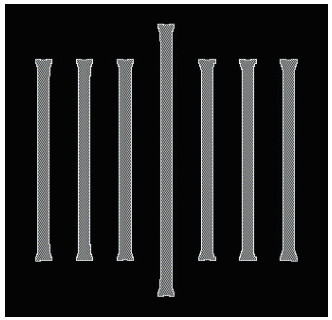
Predictive modeling involves building physically based and separable models for all elements of the patterning process.

Virtual Patterning Flow

Runtime Comparison
(932 Patterns, ~0.5x0.5μm^2 ea):

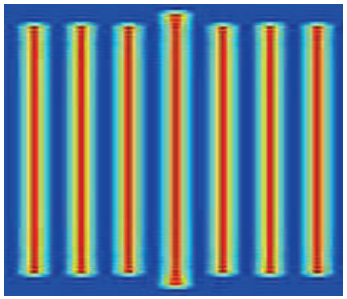
Blue Gene	12 hours
Commercial Simulator	5760 hours (8 months!)

GDS Layout



OPC Model Calibration Patterns

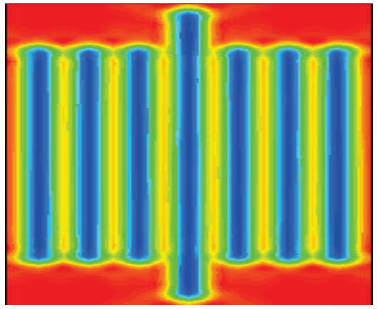
Mask Output



Rigorous EMF Modeling

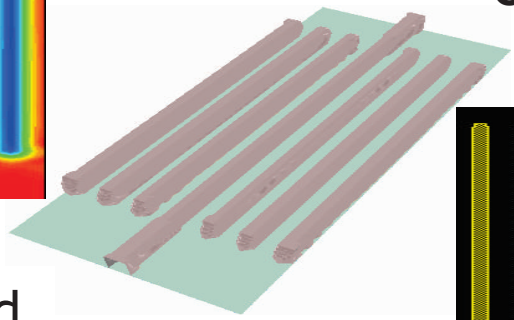
BLUE GENE

Aerial Image

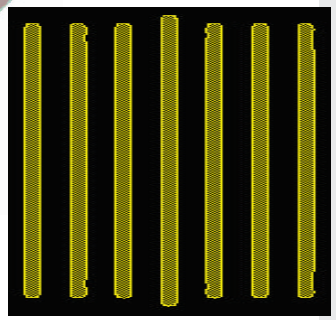


Simulated Resist CDs

Resist Profile



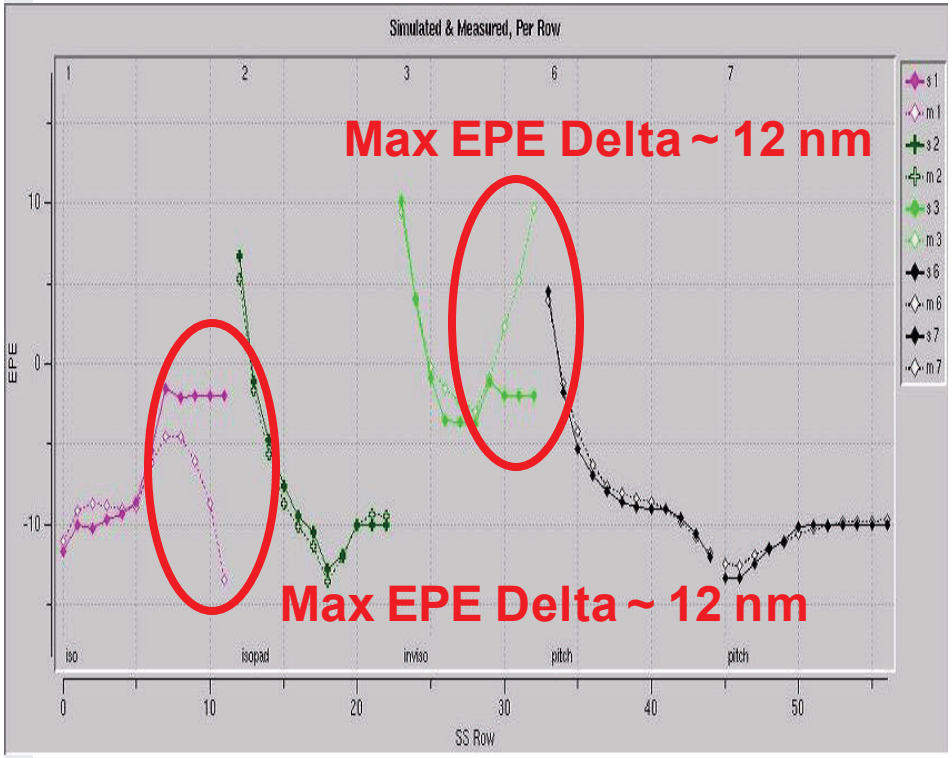
OPC Model Output



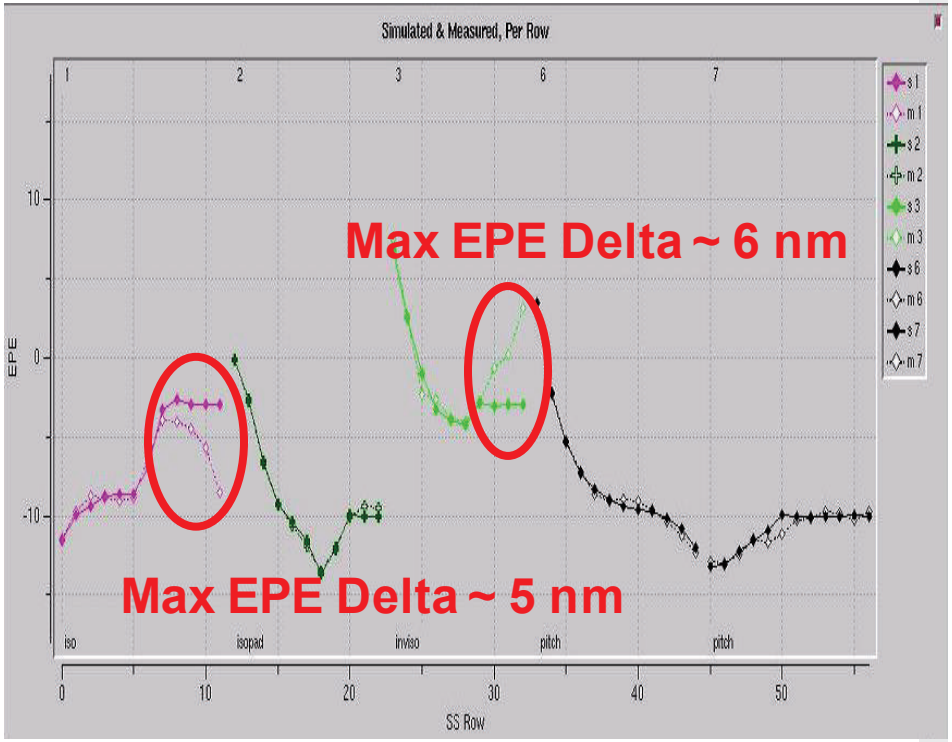
OPC Model Calibration with Simulated Data

Mask Modeling

OPC fit without Mask Model



OPC fit with Mask Model

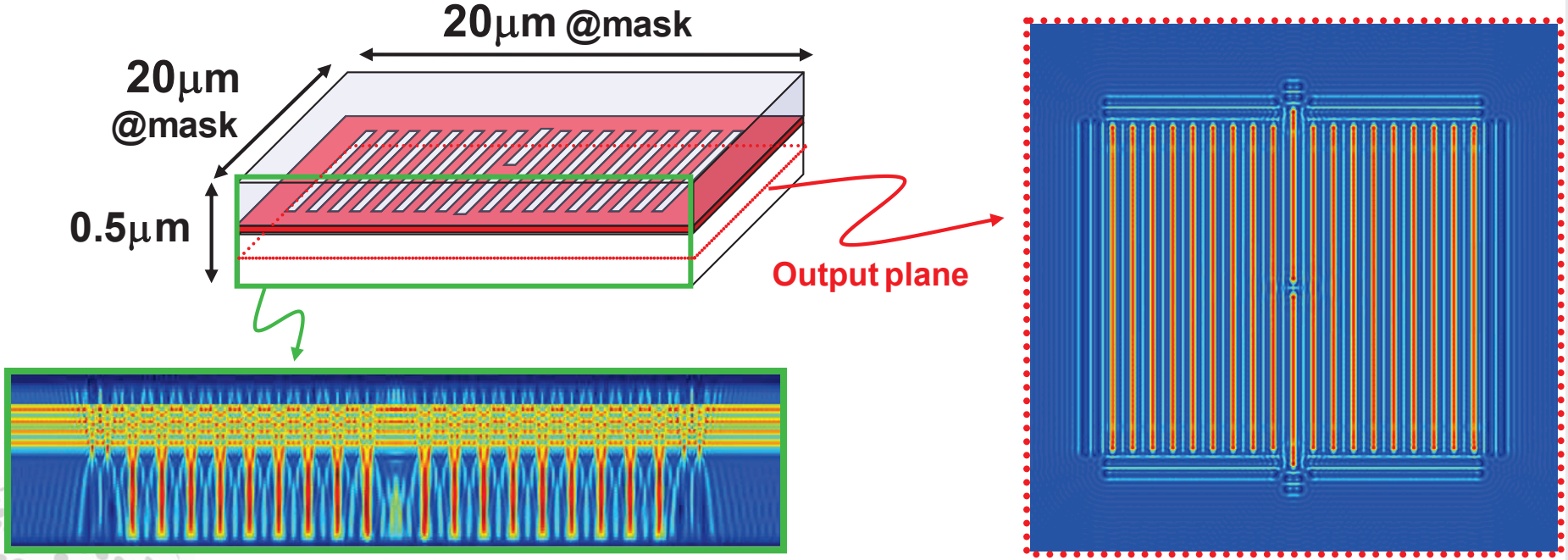


The model does not predict the data in the “red circled region” very well.
Using a mask model cuts the errors in half.

Integration of the retical systematic CD errors into an OPC modeling and correction
Geng Han, Scott Mansfield, and Azalia Krasnoperova
Proc. SPIE **6154**, 61543I (2006)

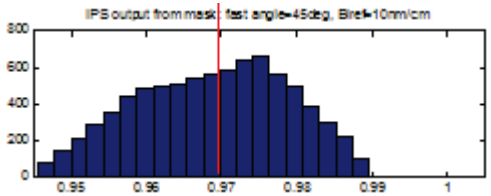
EMF Modeling

- EMF corrections are required to achieve CD tolerances
  - Traditional, simple biasing will be insufficient for future nodes
- Rigorous modeling has been computationally prohibitive
- Large area modeling addressed with internal code on Blue Gene™

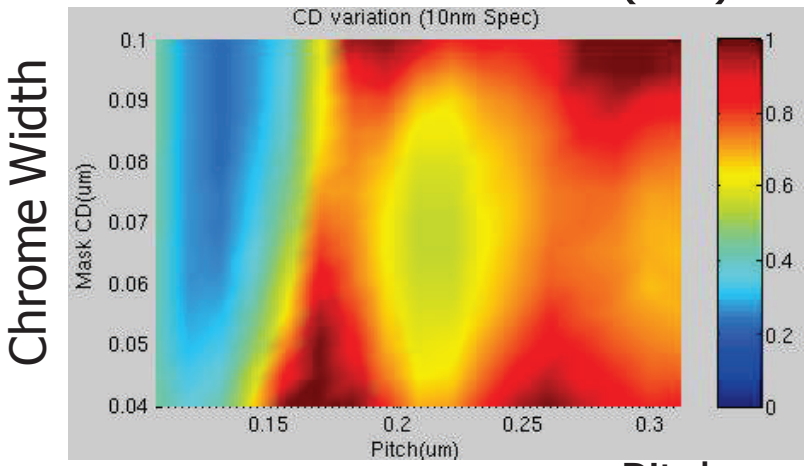


CD Sensitivity to Mask Birefringence

Δn = 10 nm/cm



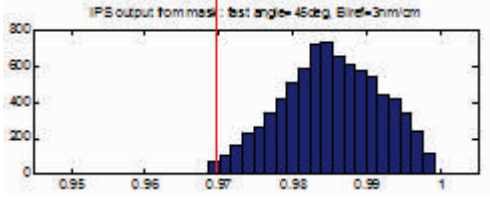
Wafer CD Variation (nm)



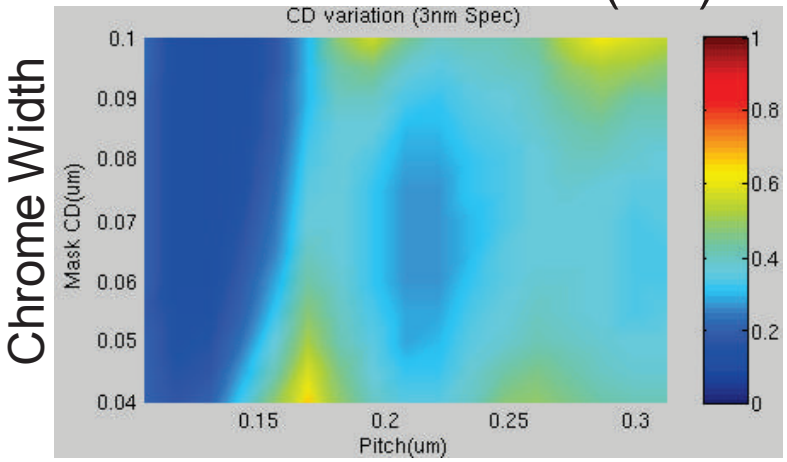
Pitch

1.2 nm max

Δn = 3 nm/cm



Wafer CD Variation (nm)



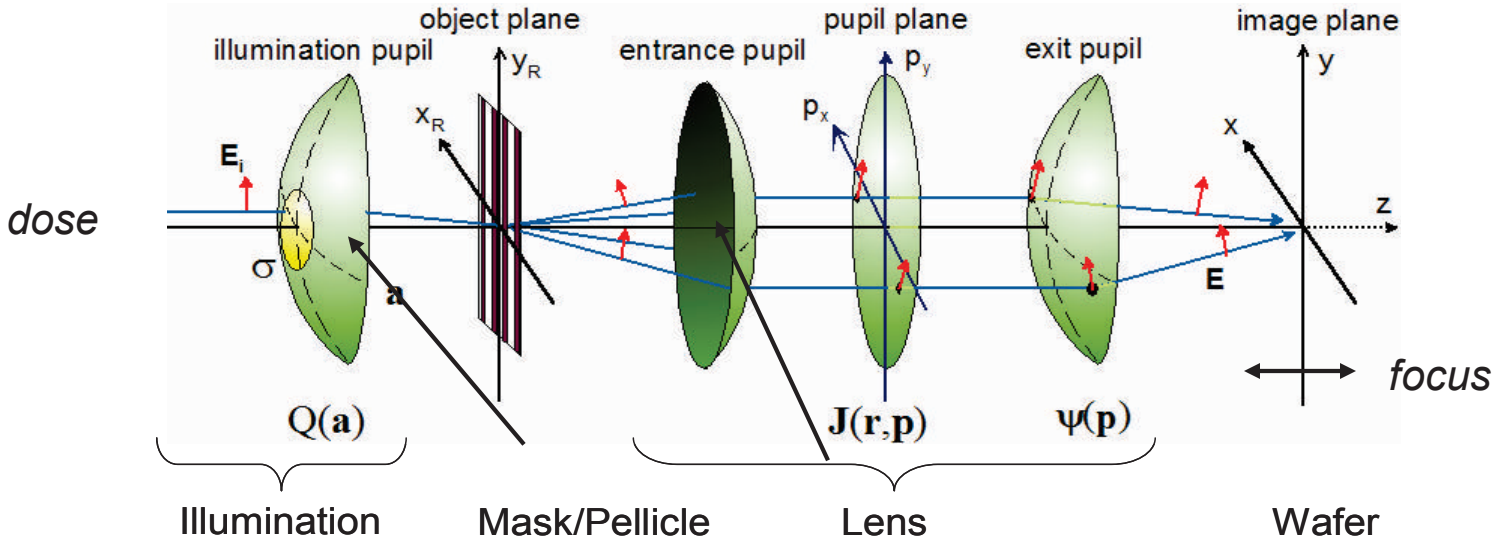
Pitch

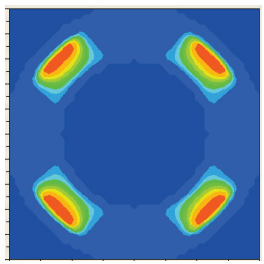
0.60 nm max

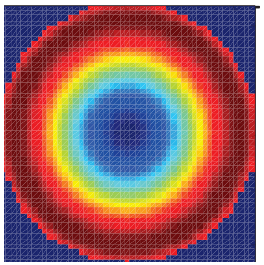
EMF simulations show the impact of mask birefringence on wafer CD uniformity.

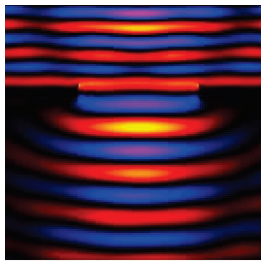
Optical Modeling

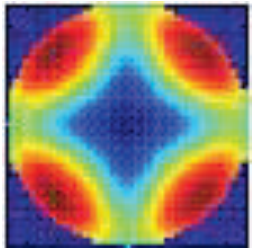
- Utilization of physical parameters whenever possible
- Goal is to have fully physical optical model

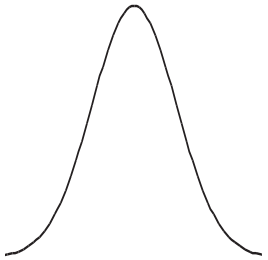



Source Map


Pupil Polarization

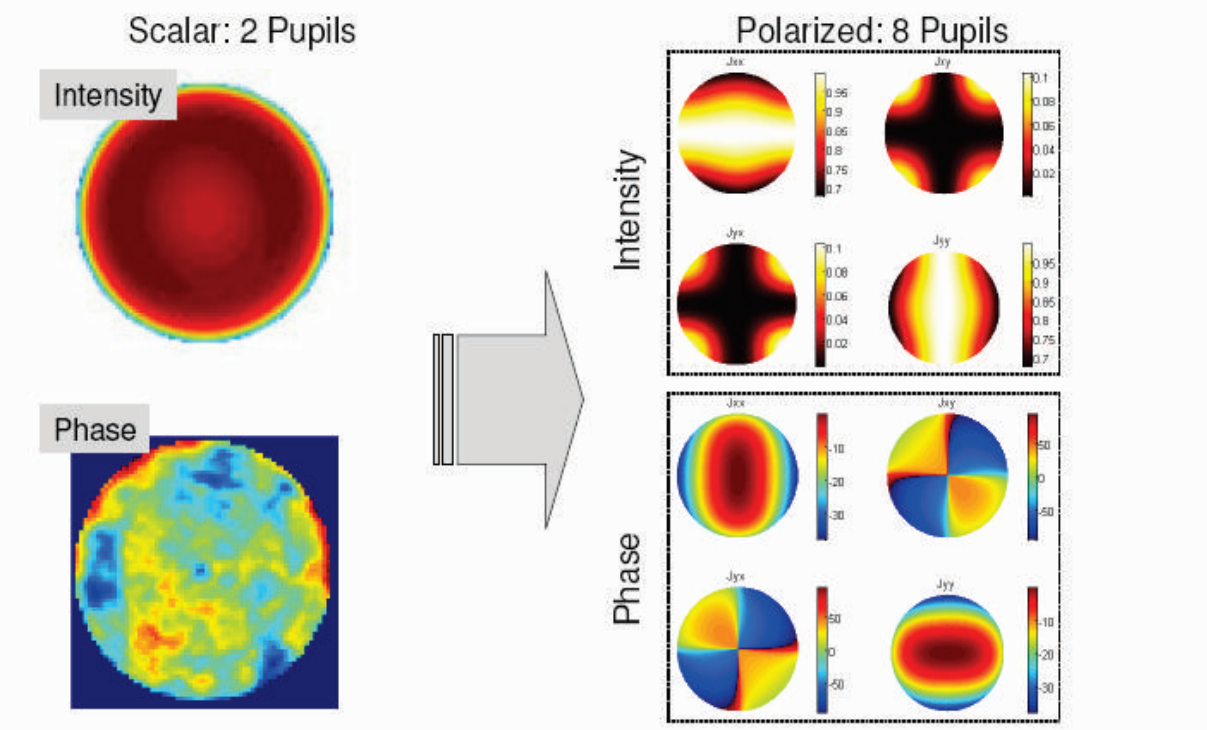

3D Mask Effects


Jones Pupil


Laser BW / Focus Blur

Hyper-NA Optics

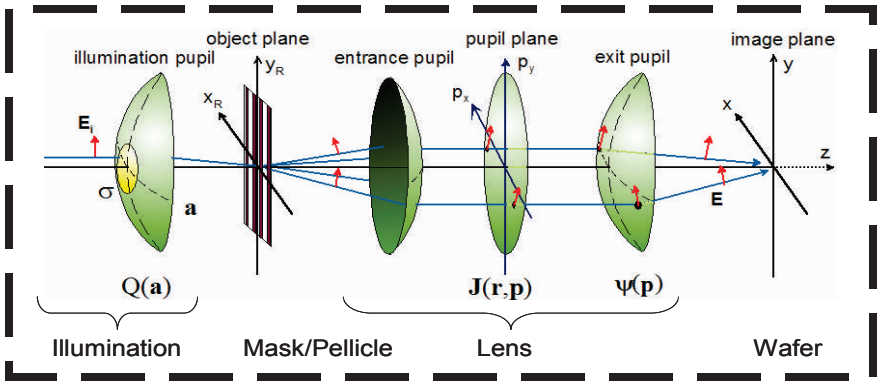
- IBM defined a convention to treat polarization for projection systems that has been adopted by the industry



Jones Matrix Convention

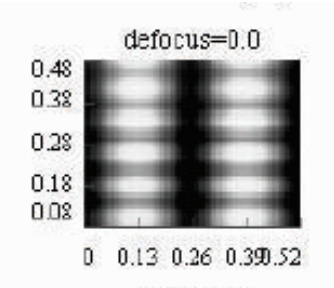
Photoresist Modeling

- Highly accurate, physically-based optical models lead to predictive resist models with few fitting terms

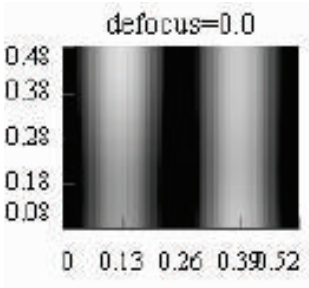


Calibration of OPC models for multiple focus conditions
Jochen Schacht, Klaus Herold, Rainer Zimmermann, J. Andres Torres, Wilhelm Maurer, Yuri Granik, Ching-Hsu Chang, G. Kuei-Chun Hung, and Benjamin Szu-Min Lin
Proc. SPIE **5377**, 691 (2004)

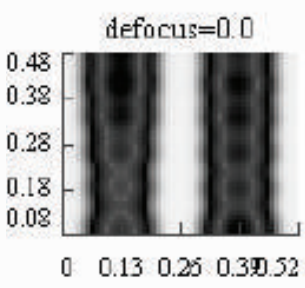
- Physically based photoresist models predict exposure and development



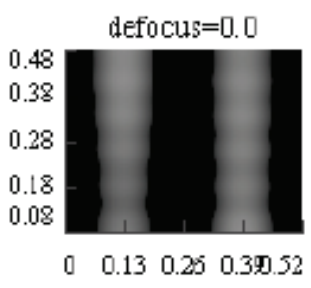
Acid Concentr before Diffusion



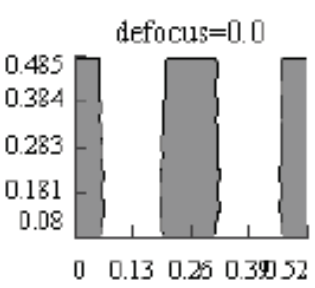
Acid Concentr after Diffusion



Normalized Deprotection



Development Rate

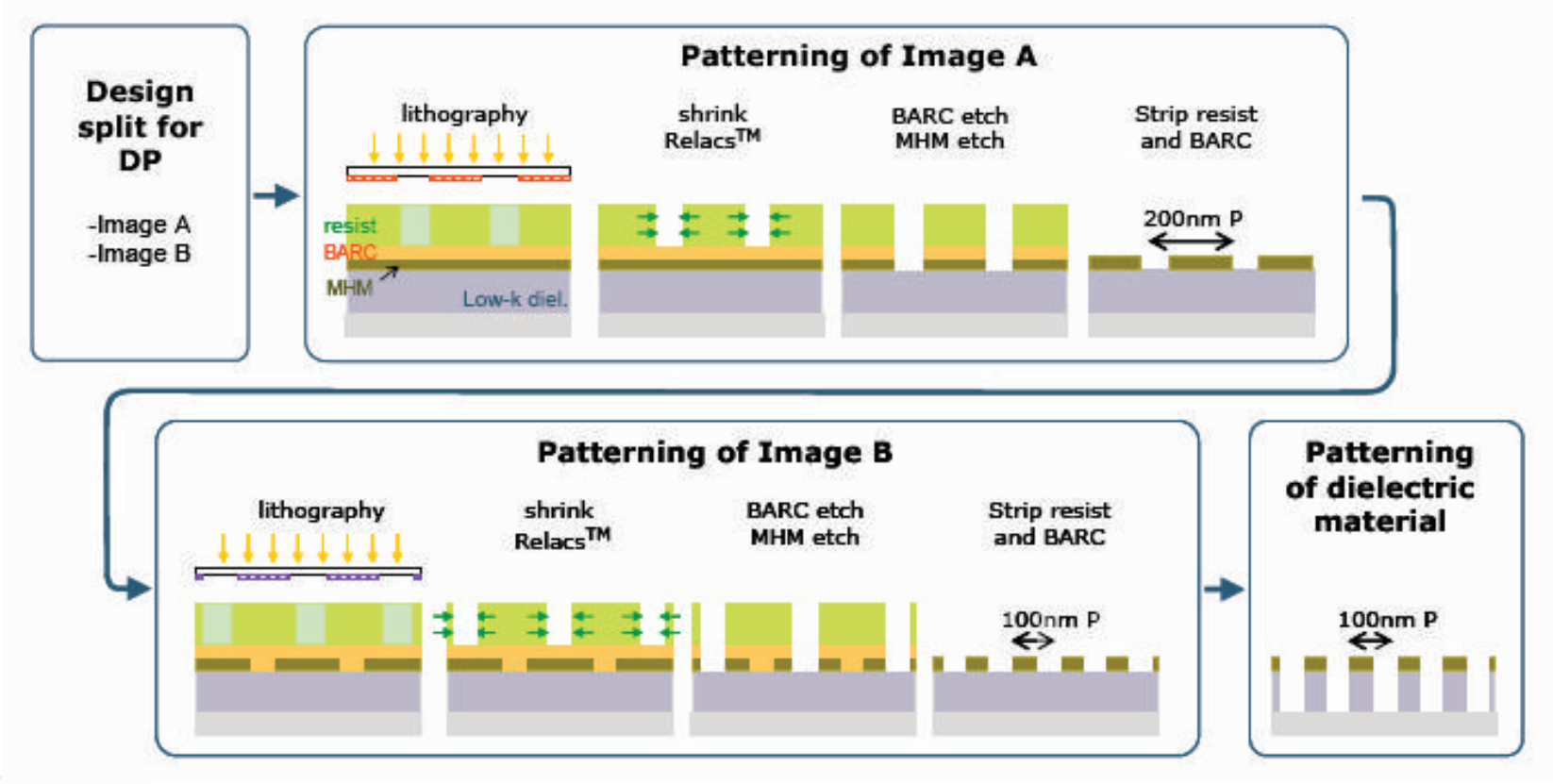


Development Contours

http://www.panoramictech.com/Products/Resist/PanoramicResistSimulator.pdf

Modeling in Double Patterning

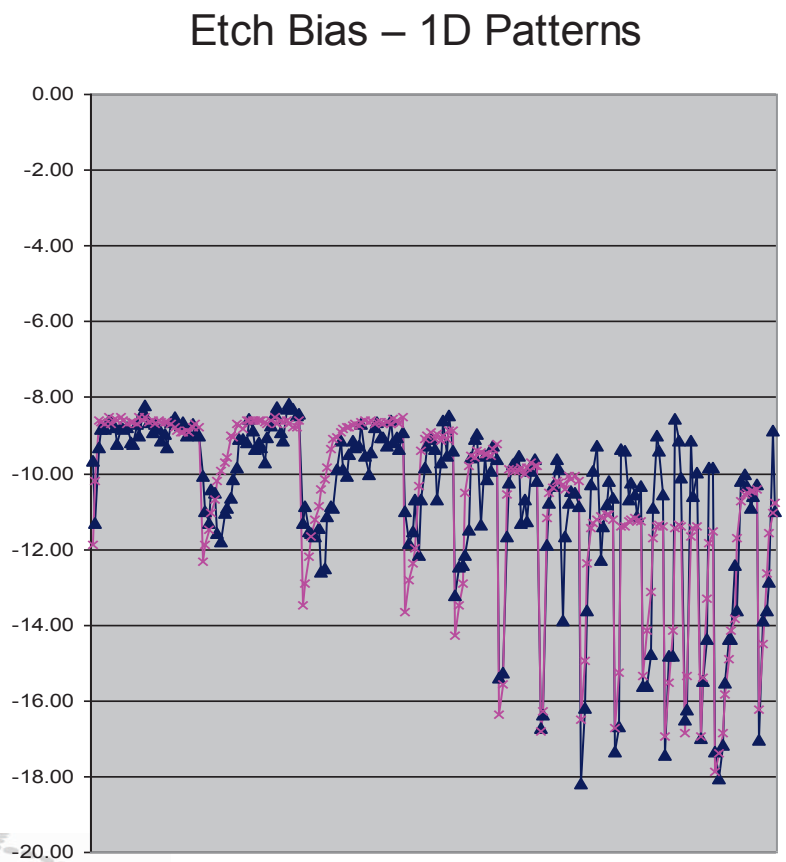
- Nonlinear shrinking techniques may be applied between lithography and etch.
- These processes must be properly modeled.

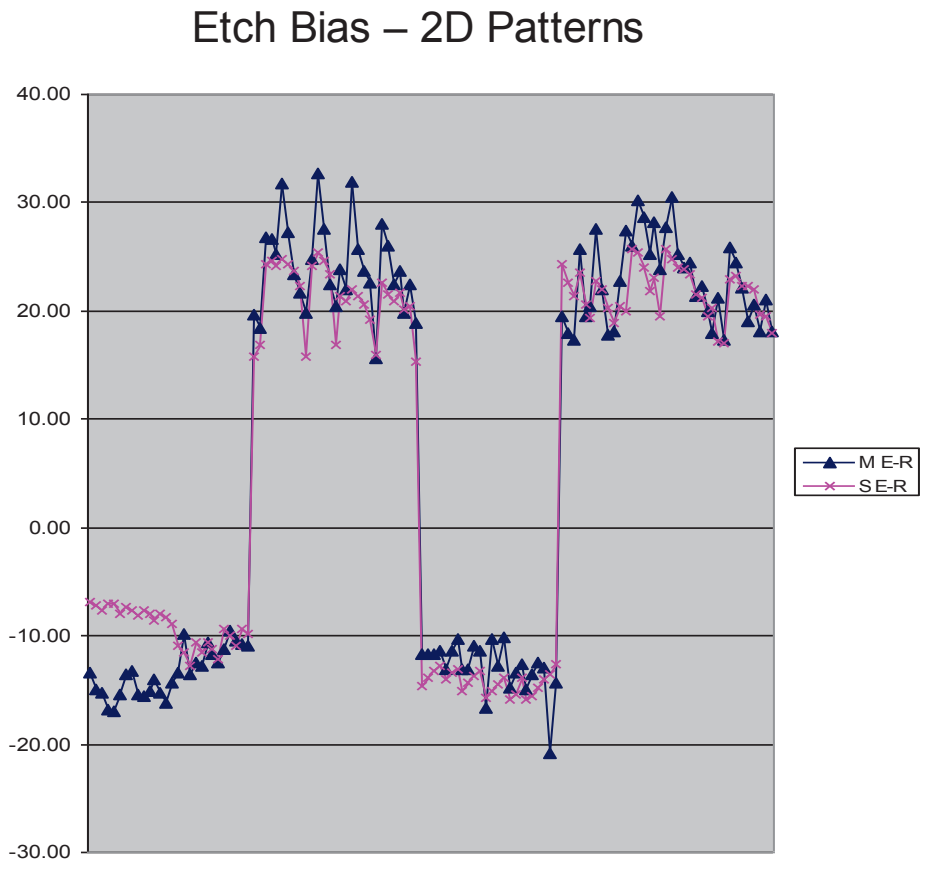


Manufacturability issues with double patterning for 50-nm half-pitch single damascene applications using RELACS shrink and corresponding OPC
Maaike Op de Beeck, Janko Versluijs, Vincent Wiaux, Tom Vandeweyer, Ivan Ciofi, Herbert Struyf, Dirk Hendrickx, and Jan Van Olmen
Proc. SPIE **6520**, 65200I (2007)

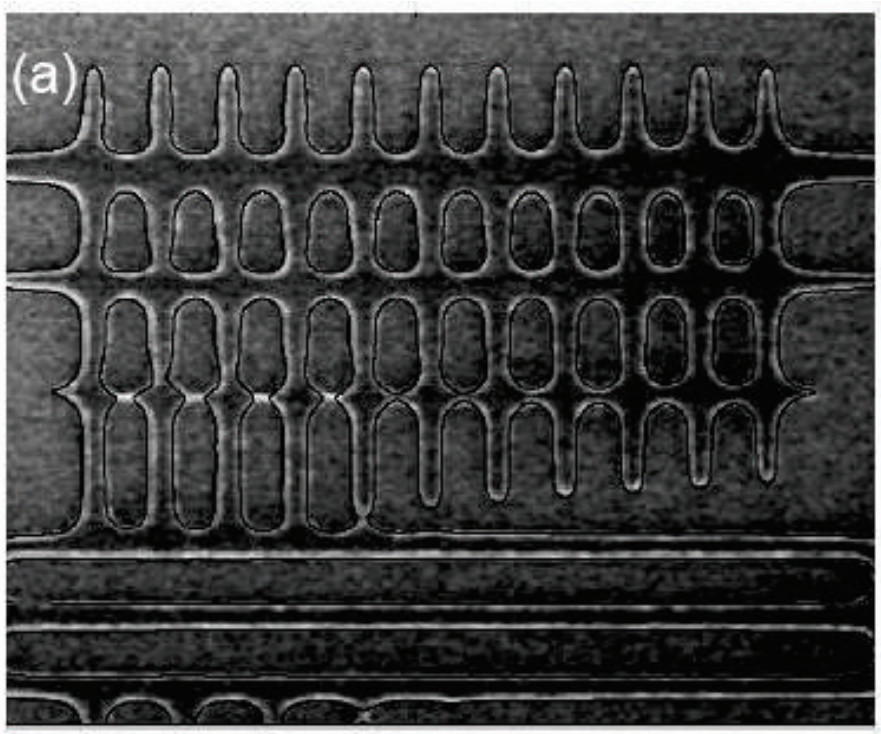
Etch Modeling

- Etch process can be effectively modeled with empirical models.

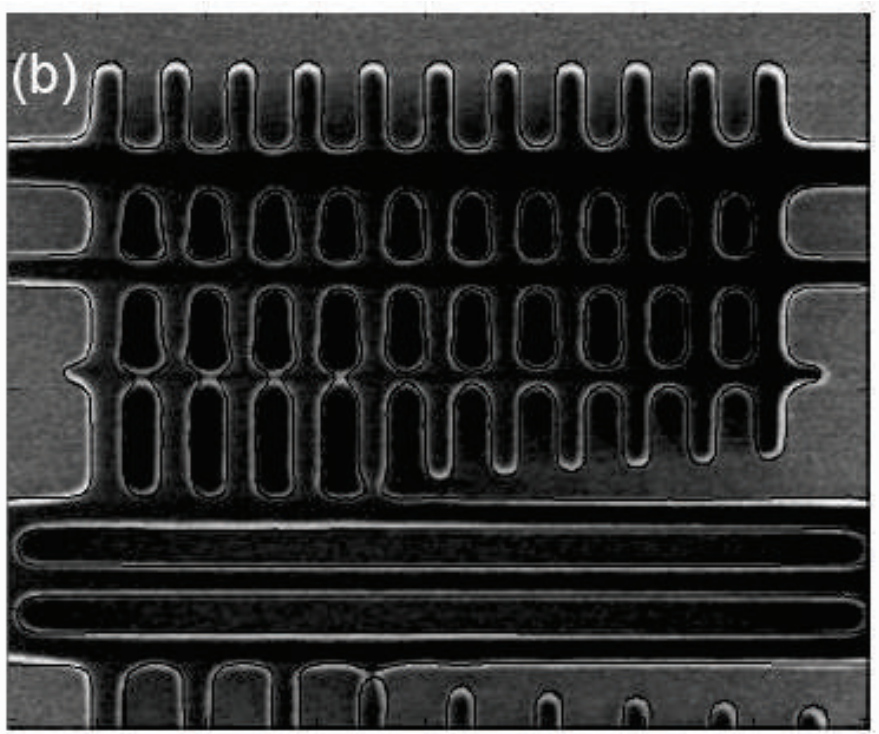




Etch modeling example



Post develop verification



Post etch verification

PPC model build methodology: sequential litho and etch verification
Ali Mokhberi, Vishnu Kamat, Apo Sezginer, Franz X. Zach, Gökhan Perçin, Jesus Carrero, and Hsu-Ting Huang
Proc. SPIE Vol. **6349**, 63491Z (Oct. 20, 2006)

Thank You