Broadband microlithography: process development using PROLITH simulator

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ABSTRACT

It was demonstrated that Optical Lithography simulations can be used very effectively for broadband application and they are not the forte of I-line lithography. PROLITH simulator was used to optimize the photo process on Ultratech 1500 broadband stepper. More than 40 process variables were required to customize the software for this process. To do a broadband simulation the optical parameters of photoresist should be measured accurately on multiple wavelengths. This information not always available from photoresist vendors and often tedious to obtain by means of UV spectroscopy. To do the final tune up the resist Exposure Rate C was scaled by the same factor N within the entire illumination range of 380-450 nm to match the experimental Dose-to-clear value E_o. Good agreement with experimental data was achieved on different device layers. Process window for the critical geometry was calculated based on the linewidth and sidewall angle specifications. Better understanding of the process allowed us to qualify new process into production in very short time frame and saved a lot of test wafers. Further process optimization is under way and efforts are being made to identify the optimum process for the future devices with smaller CDs.

Keywords: microlithography, photolithography simulation, broadband stepper

1. INTRODUCTION

TMOS devices we produce are very sensitive to photoresist profile. While investigating the resist profile from Ultratech stepper we found it to be within the range of 72 and 78 degrees. Our devices prefer a steeper wallangle. So to optimize the photo process we used PROLITH/2 Lithography simulator, that was of great help.

We tried to customize the software for our particular process which uses OCG6512 positive resist and UT1500/1.2μ stepper to verify agreement between simulations and real data. Over 40 process parameters were actually required to run the simulation. But some parameters were not readily obtainable.

- Historically PROLITH/2 was applied primarily for single (G- or I-) line steppers and broadband application have remained largely unexplored. With a broadband exposure tool, the simulator will have to use the spectral illumination output file in conjunction with resist sensitivity and bandwidth parameters (see Figure 1). Thus, all optical resist parameters (Dill parameters ABC) should be measured accurately on multiple wavelengths. This information is seldom being provided in full by resist vendor and often tedious to obtain by means of UV spectroscopy.
- In our process local resist thickness variations across the wafer as small as 0.03μ can cause the energy coupled into resist film to change by 18%, the amount that is comparable with entire process exposure latitude. That had limited the usefulness of UV spectroscopy and DRM measurement techniques.
- Probe being used in the fab to measure light intensity on stepper didn't match the meter was used by resist vendor when he measured ABC parameters.
- For OCG6512 resist PROLITH Software package came with one set of develop parameters which worked for low-normality developers only but did not describe our process which uses the HPRD486 high-normality (N=0.279) developer.

Factors mentioned above and a few other reported elsewhere [1] were accounted for model simulation mismatching the experimental CD and sidewall angle measurements.

2. EXPERIMENTAL CONDITIONS

To obtain the actual Eo values the bare Si wafers were coated with OCG6512 positive resist at a thickness varying within 1.0-1.45μ range, exposed with a boustrophedonic Dose pattern in which dose was incrementally increased with each step and developed using our standard manufacturing recipe (see Table below). IVS-100 automatic CD measurement tool was used to measure the CDs after develop while the Cambridge 240 SEM was used for CD verification and for the sidewall angle measurements. Measurements were performed on the device structures as well as on the CD targets, the 0.9 - 1.4μ CD range was investigated in this study.

Coat/Develop Process:	DNS-60A track, 6 inch wafers
HMDS prime:	in-line hot plate, 20"/30"/20" @120°C
Resist:	OCG HiPR6512, 1.22μ thickness
Coat cycle:	reverse dynamic dispense from at 100 rpm for 3 sec., 3.5 ml 21°C, 24 sec spin @ 4500rpm
Soft Bake:	60 sec. hot plate (proximity) bake @ 105°C
Thickness measurements:	PROMETRIX SpectraMap SM200/e, 121 sites
Exposure:	UT1500/1.2μ stepper, broadband, NA=0.24 E1:1 = 180-220 mJ/cm2
PEB:	in-line hot plate 60 sec. @ 115°C
Development:	HPRD486 Olin Hunt developer (0.279N TMAH), 10 sec DIW prewet, SI dynamic dispense, 28 sec. puddle time, 17 sec Rinse

3. MODEL TUNE UP

For OCG6512 resist PROLITH Software package came with just one "native set" of develop parameters which worked for low-normality developers only. For HPRD486 high-normality (N=0.279) developer we had to do DRM measurements using PE-DRM rate curve and then fit data to Mack model (Figure 2). G-line exposures were used at these measurements and data were extrapolated to broadband exposure case, a technique which validity is still remains to be seen. In addition, measurements on the PE-DRM tool were performed using the immersion type development while the puddle develop is used on DNS-60A tracks and therefore these data were not very reliable for the track-based technique. In spite of the fact that the resist's first Cauchy coefficient was adjusted 5% down to match the phase shift to the experimental E_o swing curve in-line with technique proposed in [1] somewhat data mismatch in the E-axis was still observed (Figure 4). To do a final tune up exposure rate parameter C had to be adjusted within the entire stepper illumination range of 380 to 450 nm to match the experimental Dose-to-Clear value E_o. It has been accomplished in a couple iterations with resist sensitivity C was scaled by the same factor N within the entire range of 380-450 nm. For each simulation it took a several hours to complete, much longer that a similar run for the single wave-length stepper would have taken. No attempt was made to adjust resist relative spectral sensitivity or the size of stepper bandwidth.

The resulted spectral sensitivity C was increased by 37% (Figure 3) compare with the build-in input OCG6512 file and the resulted match to experimental data is shown on Figure 4.

4. RESULTS

The SEM results for sidewall angles are shown in Figure 5 measured at -1, 0,+1 focus offset.
Simulation were done to find optimum process condition to improve the resist profile. The simulation shows that the sidewall angle is greatest when a focus offset of 0.0 μm is used, at any of the given exposures (Figure 6). The predicted range is, for the most part, the same as that of the actual samples. Thus, the model well represents the actual data.
The resulting profile is shown in Figure 7. Stages of resist profile with increasing develop time are exhibited by solid lines (top), while the highlighted area is the final profile expected when development is complete. The particular area shown below was exposed at 200 mJ/cm^2 and a focus offset of 0.0 μ. The standing wave effect can be seen on the background was occurred due to insufficient PEB.
Focus-Exposure matrixes were performed on Si, a-Polysilicon, Thermal Oxide and ILD substrates and resulted Bossung curves are shown on Figure 8. Predicted CDs were in a fairly well agreement with experimental data within the practically important Focus offset range ±4.0μ.
The model was also used to pinpoint the optimum photoresist for our process. The Shipley SPR3612 resist (Figure 9-bottom) was evaluated in the similar manner and process window was compared vs. one for OCG (top). More robust process within Fab process specification (CD = 1.2μ ±10%, sidewall angle > 76°, resist lost <10%) and 33% nominal exposure dose $E_{1:1}$ reduction can be achieved by switching to Shipley SPR3612 resist.

Another important question one can ask in practical photolithography is what a minimum geometry can be achieved with the current well established process and what would the process window look like if a new more advanced stepper was used ? This is valid when technology evolving mainly by shrinking the die size without a major device redesign and to implement the advanced I-line stepper can be cost prohibitive. To benchmark the process at another fab or at the vendor facility is not always possible, but mistakes associated with a wrong exposure tool choice are always costly. Here a fine tuned model comes very handy. In was predicted that the SATURN broadband stepper can deliver some improvement as far as a sidewall angle window, but at the expense of a lesser depth of focus (Figure 10). Though the resist profile at the focus position and at the nominal exposure dose look much steeper (Figure 10, bottom) compare with UT1500 (top) the image will degrade faster with a focus offset increase. The bandwidth on the SATURN is shifted toward I-line while Numerical Aperture NA is increased up to 0.365 and according to the Rayligh criteria [1] the Depth of Focus can be estimated as:

$$\mathbf{DOF = k\lambda/NA} \qquad (1)$$

where **k**, the process dependent coefficient. **k** is typically in the range of 0.7 to 1.0 in the manufacturing environment.

Depth of Focus is reduced almost by half when the same resist process is used. On the other hand, the 0.9-1.0μ process can be performed on the SATURN stepper at the higher photospeed, with OCG6512 dual-line resist some 10% below the current nominal dose.

5. CONCLUSIONS

It was demonstrated that Optical Lithography simulations can be used very effectively for broadband application like Ultratech stepper. They are not the forte of I-line lithography. Good agreement with experimental data was achieved not just for the bare Si wafers but for other device layers as well. Process window for the critical 1.4μ geometry (WAVEFET) was measured based on the linewidth and sidewall angle specs. Better understanding of the process allowed us to qualify new devices into production in very short timeframe and saved us numbers of test wafers otherwise would be necessary to run in qualification tests. Further process optimization is under way and attempt is being made to evaluate the optimum process for the future generations of devices with a smaller CD.

ACKNOWLEDGMENTS

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REFERENCES

1. Stephen Thornton, Chris Mack, "Lithography model tuning: matching simulation to experiment", SPIE, vol. 2726 (1996)
2. PROLITH/2™ is a trademark of FINLE Technologies, Inc.

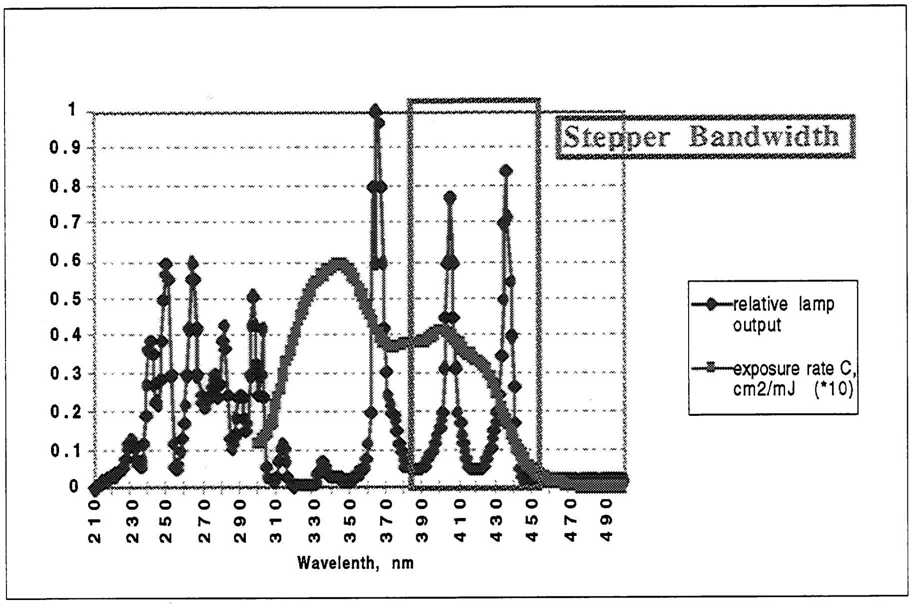


Figure 1. UT1500 illumination output and OCG6512 photoresist Exposure rate

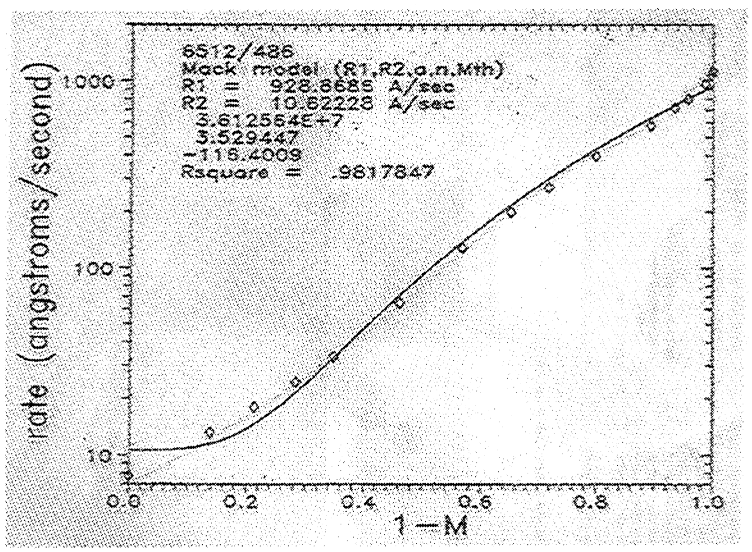


Figure 2. DRM data for OGG6512/HPRD486

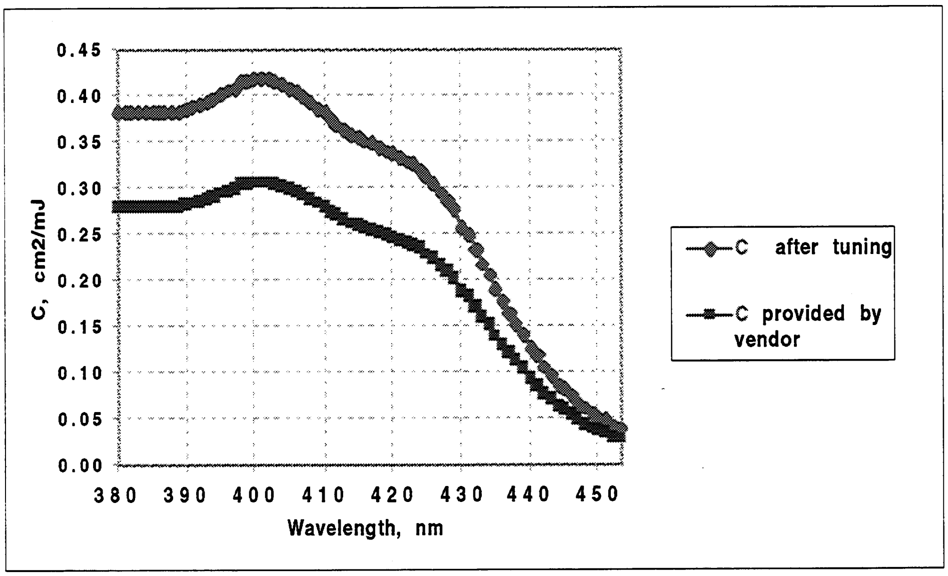


Figure 3. Exposure rate for HiPR6512 resist in UT1500 exposure range: initial and adjusted

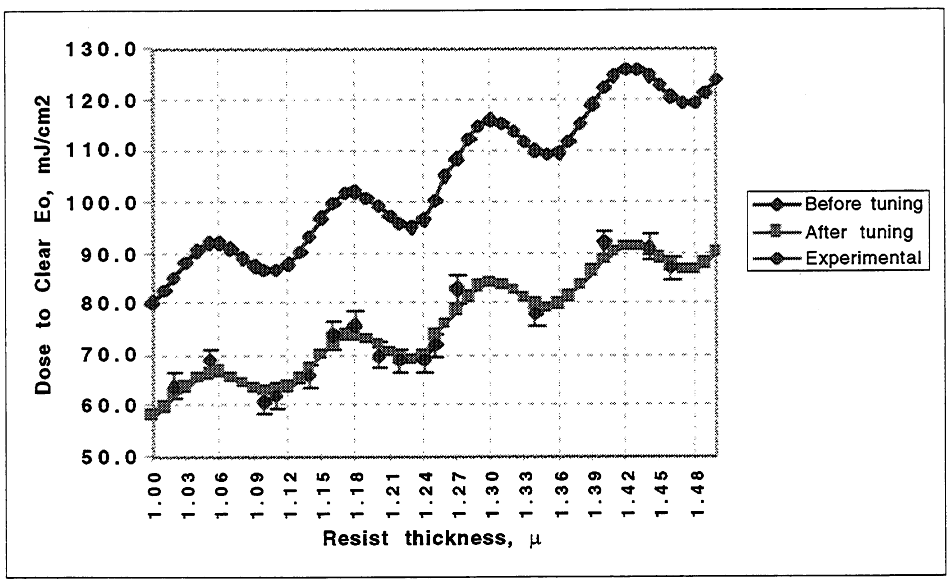


Figure 4. Eo swing curve: simulation and experimental data

	Slope Angle, °		
Exposure Energy	Focus Setting, [μ]		
[mJ/cm^2]	-1.0	0.0	1.0
150	73	74	73
200	74	77	75
250	75	78	76

Figure 5. Slope Angle values (Cambridge 240 SEM).

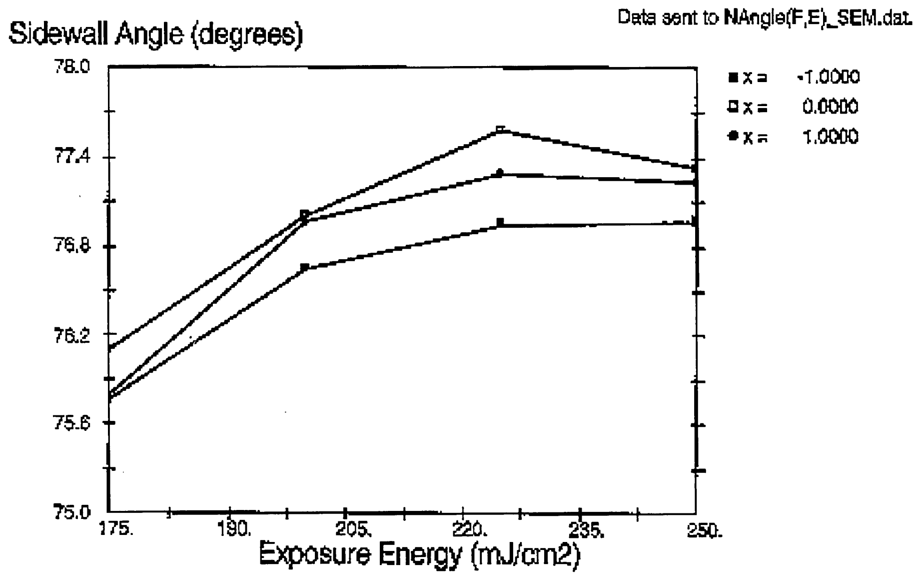


Figure 6. Slope Angle as a function of exposure/focus set up (PROLITH simulation)

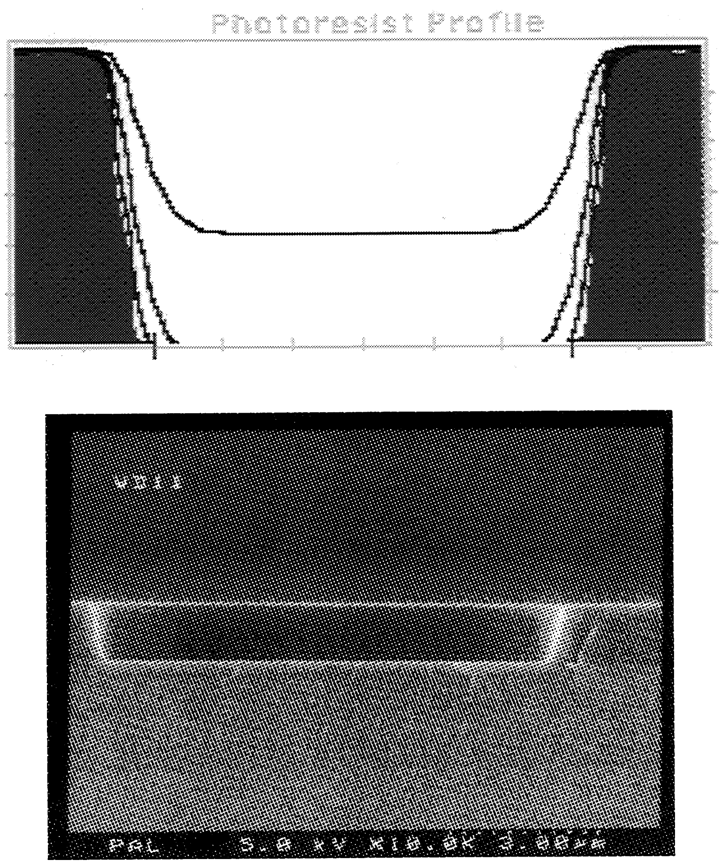
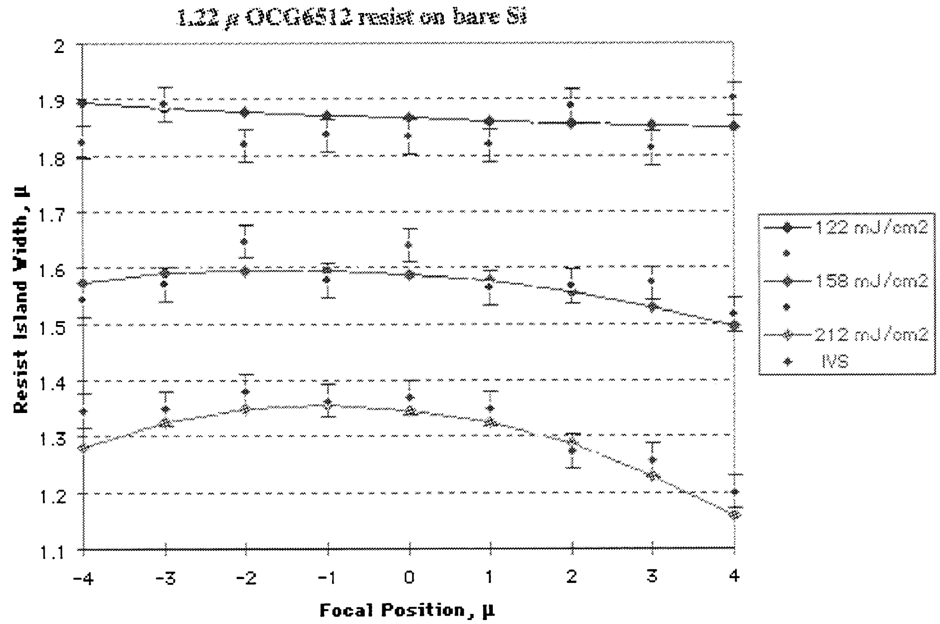


Figure 7. Resist Profile: PROLITH/2 simulation vs. SEM.



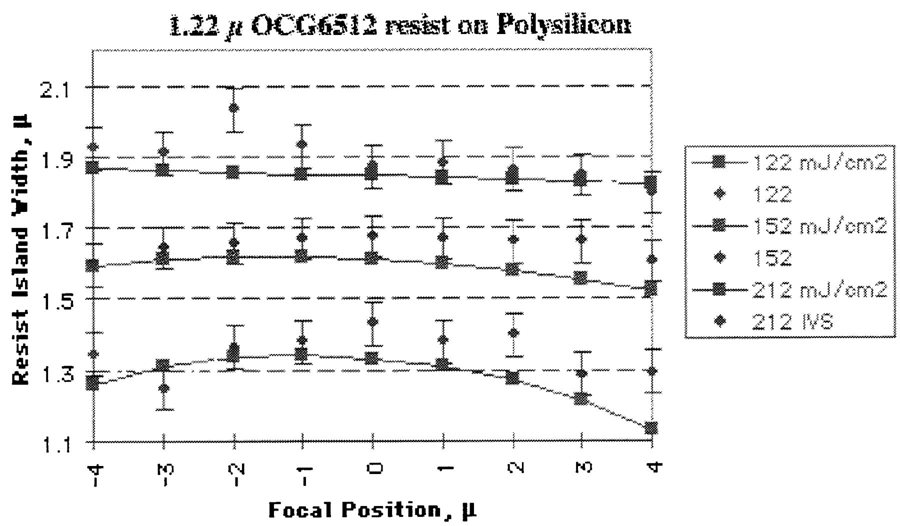


Figure 8. Bossung curves for OCG6512 resist on the Silicon substrate (top) and Poly-silicon (bottom).

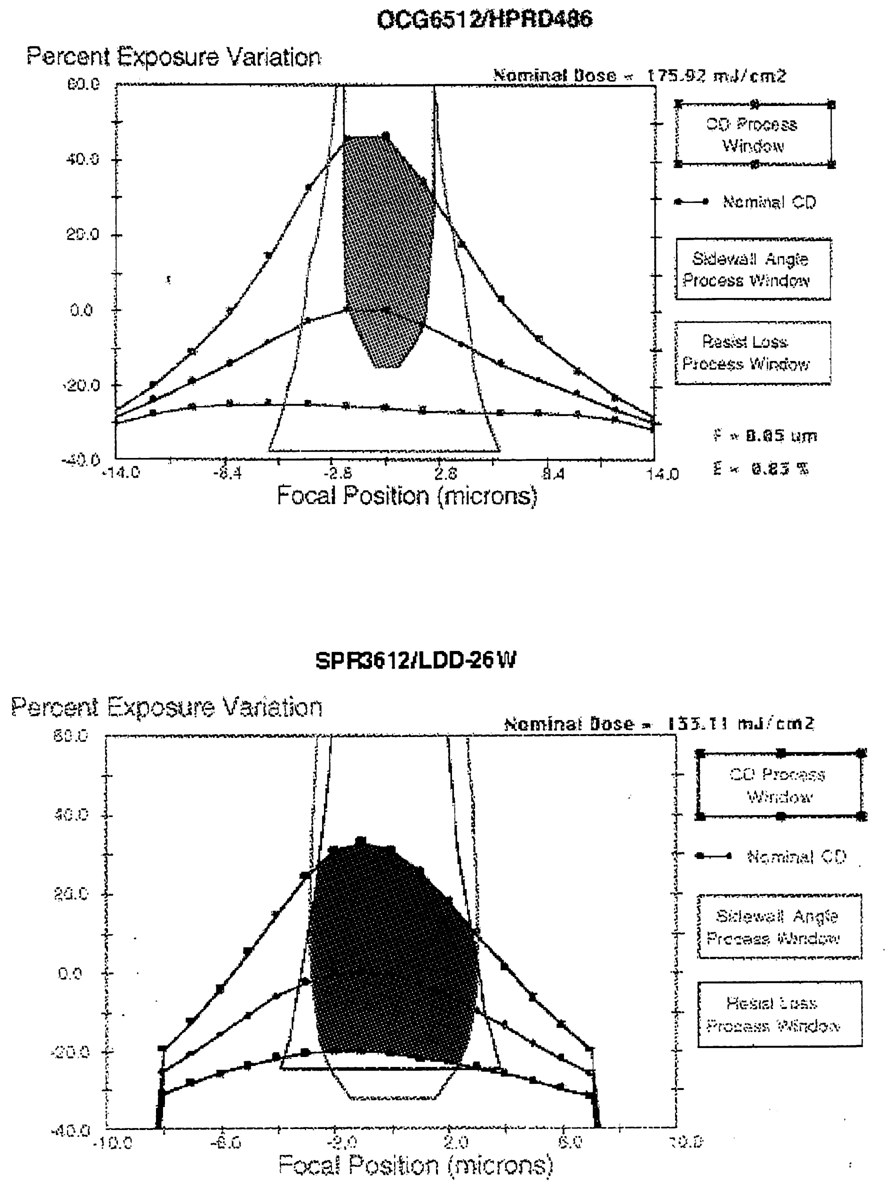
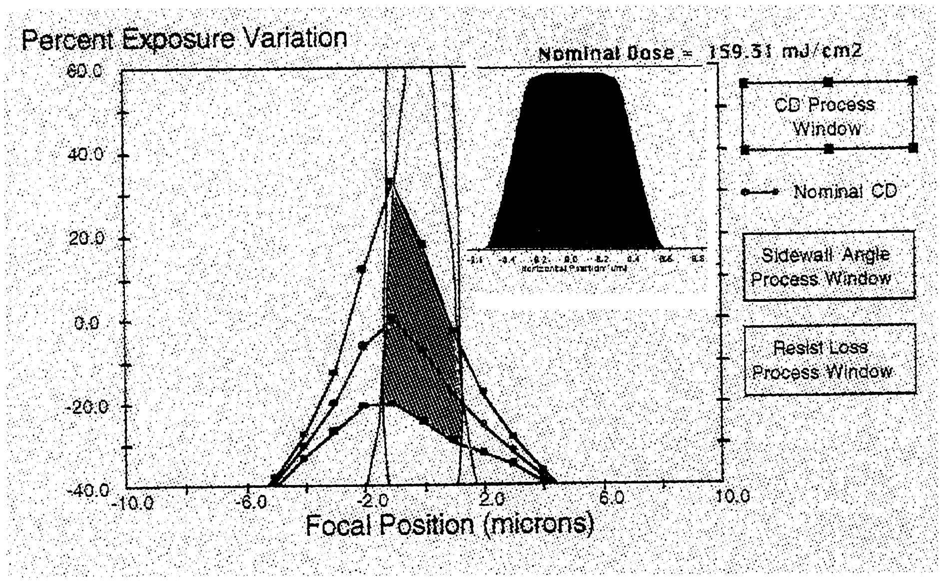


Figure 9. Process window for OCG 6512 (h=1.22μ, top) vs. Shipley SPR3612 (h=1.21μ, bottom). N+Block mask, CD target =1.2μ.



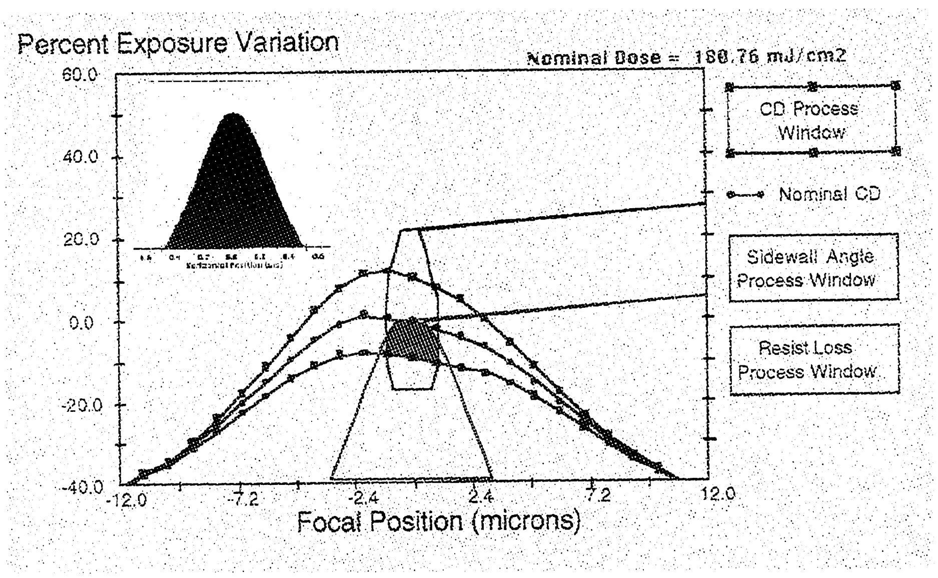


Figure 10. Process window on the UT1500/1.0μ stepper (top) compare with one calculated for the SATURN (bottom). OCG6512 resist, h=1.22μ. N+Block mask, CD target = 0.95μ. Resist profiles are shown calculated at the nominal Exposure Dose.