Consultant Curriculum Vitae

Vojin G. Oklobdzija, Ph.D., IEEE Life Fellow

Professor Emeritus, University of California
Past-President, IEEE Circuits and Systems Society, 2014, 2015
(Phonetic spelling: Vo-in Oklob-j-a)

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Expertise

- Computer System Design and Computer Architecture
- VLSI Circuits and Systems
- System Clocking and Clocked Storage Elements
- Logic Design and Machine Organization
- Low-Power Design and Technology
- Computer Arithmetic: VLSI adders, multipliers arithmetic, crypto processors
- Microprocessor Design
- Design for Testability and Fault-Tolerant Computer Design

Professional Summary

Expert witness with 25 years of experience, provided testimony in civil jury trial, and ITC court in Washington, D.C. Provided deposition testimonies, written over 30 expert reports on infringement, claim construction, participated in patent review.
Over 50 years of experience in computer and semiconductor industry and 35 years of consulting experience for most major computer and semiconductor companies in the USA and abroad.
Twenty years in academic position, reaching the highest Full Professor level in five years and IEEE Fellow, followed by IEEE Life Fellow (highest) level in engineering profession.

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Education: Vojin G. Oklobdzija

Year	College/University	Degree
1982	University of California at Los Angeles	Ph.D., in Computer Science with Minor in Electronics
1978	University of California at Los Angeles	MS, Computer Science with thesis in Computer Arithmetic
1971	University of Belgrade, Yugoslavia	Ms. E.E. (Dipl. Ing) Electronic and Telecommunications
1968	University of Belgrade, Yugoslavia	BS. E.E. (Ing) Electrical Engineering

Professional Associations and Achievements

- Fellow of the Institute of Electrical and Electronic Engineers, since 1996[1].
- Life Fellow, IEEE since 2016[2].
- Member, Japan IEICE Society.
- Fulbright Scholar 1976.
- Fulbright Professor, Peru 1991.
- Fulbright Professor, Argentina, 2013.
- President: IEEE Circuits and Systems Society (2014-2016 two-year term).
- President Elect, IEEE Circuits and Systems Society (2013).
- Vice President, Technical Activities, IEEE Circuits and Systems Society (2009-2013).
- Board of Governors, IEEE CAS, 2010-2016.

Award and Recognitions

Fulbright Scholarship, 1976-77.
National Science Fellowship, Plasma Physics, 1971-73.
IBM patent award, 1985.
IBM invention plateau award, 1985.
Best Paper Award in Computer Architecture track, HICSS-88.
Fulbright Professorship, 1990. Peru, South America.
Fulbright Professorship, 2013. Argentina.
N. Price Fellowship in Electrical Engineering, Australia 1993.
Fellow IEEE, 1995.
Distinguished Lecturer of IEEE Circuits and Systems Society.
Distinguished Lecturer of IEEE Solid-State Circuits Society.
Outstanding Academic Title, "Computer Engineering Handbook," CRC Press 2002.
Listed in Marquis: "Who'sWho in America," "Who'sWho in Science and Engineering,"
"Clock-Powered Circuits Set Efficiency Record," Electronic Engineering Times, December 1, 1997.

[1] only less than 0.1% of 427,000 members are elected IEEE Fellows each year.
[2] the highest achievable grade, there are only 3517 total out of 427,000 members in the world.

"ISLPED '97 Shows What's Up in Ultra-Low Power Digital Systems," article mention, Electronic Design, August 4, 1997.
Active Ham-Radio operator, since 1962. Call sign WF1A, holder of the highest class.[3]

Current and Past Professional Service:

- Past-President, IEEE Circuits Systems Society
- General Chair: International Symposium on Computer Arithmetic, ARITH-20. (Tubingen, Germany, 2011)
- General Chair: Int'l Symposium on Low-Power Electronics Design, Austin, Texas, 2010.
- Technical Program Chair, Int'l Symposium on Low-Power Electronics Design, Bangalore, 2009.
- Technical Program Chair: International Symposium on Low-Power Electronics, 2008.
- General Chair: International Symposium on Computer Arithmetic, ARITH-13, Pacific Grove, California, 2007.
- General Chair 13th IEEE Symposium on Computer Arithmetic 1997.
- General Chair, 7th IEEE Dallas Circuits and Systems Workshop, 2008.
- Conference Chair: IASTED International Conference on Circuits, Signals and Systems, 2005.
- Track Chair, Logic and Memory, Int'l Conference on Computer Design, 2008.
- Program Committee Member: Asian Solid-State Circuits Conference: 2005, 2007.
- Editor, Computer Engineering Series, Taylor & Francis.
- Editorial Board Taylor and Francis / CRC Press.
- Associate Editor, IEEE Transactions on Computers: 2001-2005,
- Associate Editor, IEEE Transactions on VLSI Systems: 1995-2003,
- Associate Editor, IEEE Transaction on Circuits and Systems II: 2006-2008
- Editorial Board, Journal of VLSI Signal Processing,
- ISSCC 1997 Panel Organizer.
- Chair, ISSCC, Microprocessor Design Workshop, 2001.
- Organizer and Presenter: ISSCC, Microprocessor Design Workshop, 2002.
- Vice-Chairman, VLSI and Technology Technical Conference, ICCD-89, ICCD-90.
- Computer Architecture Mini-Track Chairman, HICSS-22, HICSS-25 and HICSS-27.
- Organizing committee Hot Chips Symposium, Stanford University, 2000, 2001
- IEEE Solid-State Circuits Society: Oakland / East Bay Chapter President: 2000-2004.
- Academic Freedom & Responsibility, Campus Committee, U.C. Davis, 2002, 2003.
- Guest Editor Journal of VLSI Signal Processing 1988.
- Member of the Board of Governors, IEEE Circuits and Systems Society (2008-2016)
- Editorial Board, IEEE MICRO.
- Editor, Computer Engineering Series, Taylor & Francis.
- Editorial Board Taylor and Francis / CRC Press.
- Distinguished Lecturer of IEEE Solid-State Circuits Society: 2000-6.

[3] Experimenting with packet radio networks, low-power signal propagation, antennas, computer-radio interfaces.

Program Committee Member:

International Solid-State Circuits Conference: ISSCC: 1996, 1997, 1998, 1999, 2000, 2001, 2007
Asian Solid-State Circuits Conference, A-SSCC: 2005.
IEEE Computer Arithmetic Conference: 1989, 1993, 1995, 1997, 1999, 2001, 2003, 2005, 2007, 2009.
International Symposium on Low-Power Electronic Design: 2001- 2008
ISCAS: International Symposium on Circuits and Systems:
PATMOS: Power and Timing Modeling, Optimization and Simulation: 2006, 2007, 2008, 2009
Asilomar Conference on Signals, Systems and Computers: 1988 – 1996.
CompCon 1989.
ICCD: International Conference on Computer Design: 1984, 1988, 2008.

Referee for:

IEEE Transactions on Computers,
IEEE Journal of Solid-State Circuits,
IEEE Computer Magazine,
IEEE MICRO
IEEE Transaction on Circuits and Systems, CAS-I,
IEEE Transactions on CAD,
IEE Proceedings
IEE Electronics Letters
FTC: Fault Tolerant Computing Symposium,
ARITH: Symposium on Computer Arithmetic,
ISCA: International Symposium on Computer Architecture.

Book Reviewer:
McGraw Hill, Prentice Hall Publishing, Oxford Publishing, Oxford University Press.
Addison Wesley Longman Publishing Group, Brooks / Cole Publishing Company.
Kluwer Academic Publishers, UVC: University Video Communications.
Cambridge University Press, review of: "*Basic Electronics and Analog IC Design*" by Sergio Franco.
Cengage Learning/Thomson Learning, reviews of: "*Computer Architecture and Organization"*

Funding Agencies:
National Science Foundation, Referee, Panel Member 2008
California MICRO,
ARC: Australian Research Counsel, Referee
Swedish Foundation for Strategic Research: Program evaluator and panel member for Microelectronics program, 2005.

Research Funding

Over 1M$ in US research funding and over 1.4M A$ in Australian Research Council funding and $700,000 equipment grant. Research supported by: IBM Corp., Intel Corp., Fujitsu Ltd.,

Marvel Corp., Silicon Systems Inc. / Texas Instruments, Hitachi Ltd. SRC: Semiconductor Research Counsel, California MICRO, NSF.
Recent Funding: *500,000A$, ARC November, 2007, 300,000$US (SRC, January 2008), $110,000 SRC 2009, $120,000 Texas SSR, $270,000 SRC 2011, $120,000 NMSU 2011.*

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Employment History:

From: 2018 **SambaNova Systems Inc.**
To: 2023 Palo Alto, California
Position: Senior Principal Engineer
Machine Learning: Processor design and development. Responsible for the Arithmetic Unit.

From: 2016 **Esperanto Technologies Inc**
To: 2018 Mt. View, California
Position: Founding Member
Massively parallel, ultra-low-power microprocessor system development. Working on low-power and low-voltage design in order to achieve minimal power operation for a given performance.

From: 2013 **Silicon Analytics Inc.**
To: 2020 San Jose, California
Position: Founder and President
Expertise and tool development for power optimization. Targeting low and ultra-low power design.

From: 2013 **Skyera Inc.**
To: 2014 San Jose, California
Position: *Senior Director, Processor Development*
Design of a massively parallel processor supporting Solid-State, Peta-Byte storage array. Managing entire processor design team.

From: 1996 **Integration Corp.**
To: Present Berkeley, California
Position: President and CEO
Processor design services: Developed fastest network encryption processor for Blue Steel Networks (sold to Broadcom for $150M). Designed and developed network encryption processor for Digital Archways. Design and developed Media and Floating-Point Processor for BOPS Inc.

From: 1992 **Advanced Computer Systems Engineering Laboratory**
To: Present Currently: Berkeley, California
Position: *Director*
Conducting research in: Low-Power systems and processor development with implementations in multi-media, cryptography and wireless communication. Developed a comprehensive family of clocked storage elements and clocking strategies for high performance and low-power applications; optimization method for digital circuits and system design resulting in up to 50% energy savings; the fastest parallel multiplier, adder and method for generation, estimation and comparison of arithmetic structures.

From: 1991 **University of California Davis**
To: Present Davis, CA
Position: Professor Emeritus, 2006-Present

1991-2006: Full Professor, Electrical and Computer Engineering Department

From: 2007 **University of Texas at Dallas**
To: 2010 Dallas, TX
Position: *Visiting Professor;* Director of Systems and Circuits Group (2007-2010), *Adjunct Professor (2010 – 2012)*

From: 2005 **Sydney University**
To: 2007 Sydney, Australia
Position: *Computer Engineering Chair and Chair Professor, Department of Electrical and Information Engineering*
(ARC funding $1,900,000).

From: 03/2004 **Ecole Polytechnique Federale de Lausanne, EPFL**
To: 10/2004 Lausanne, Switzerland
Position: *Visiting Professor, Processor Architecture Laboratory*
Developed and taught a new doctoral course in computer arithmetic

From: 07/2003 **Government of Korea**
To: 12/2003 Seoul, Korea
Position: *Distinguished Visiting Professor,* Korea Information Technology Assessment Program
Established research program in digital media and secured a three year grant in *"Power Minimization for Media Signal Processing"* from the Korean government (appx: $300,000). Established and taught the course titled: *"Digital System Engineering"*.

From: 1998 **University of California at Berkeley**
To: 1990 Berkeley, CA
Position: *Visiting IBM Faculty, Electrical Engineering and Computer Science Department*
Teaching: *Upper level courses:* CS150 Digital System Design, CS152: Computer System Design and Organization. *Graduate courses:* CS252 Computer System Architecture, CS292I VLSI Implementation of Fast Computer Arithmetic. Assisted in preliminary evaluation and preparation of Patterson-Hennessy book "Computer Architecture: A Quantitative Approach".

From: 1996 **Siemens Corporation**
To: 1998 San Jose, CA
Position: Architecture / Circuit Design Manager
Development of Full-Custom high-performance arithmetic units. Chief architect for Siemens / Infineon TriCore line of integrated RISC-DSP controller. Development of and embedded Logic-DRAM processor (32-bit, RISC + DSP). Managed a group of 15 engineers.

From: 1982 **IBM T.J. Watson Research Center**
To: 1991 Yorktown Heights, NY
Position: *Research Staff Member*

My work was in the areas of: *Systems and Architecture, CPU and Floating-Point processor design, Circuit design, Design for Testability*
Development and implementation of VLSI RISC architectures:
1. High Performance 801 (first RISC microprocessor) for PC-RT (ROMP-E project).
2. Very high performance Super-Scalar RISC Architecture, RS/6000: floating point processor and system organization. (current PowerPC architecture)
3. Architectural definition and design of VLSI-RISC type processor to be used in a highly parallel super-computer. IBM SP-2.

From: 1979 **Xerox Corp.**
To: 1982 El Segundo, CA
Position: *Member of the Engineering Staff, Microelectronics Center*
Work on the VLSI microprocessors design and diagnostic. Chip set for the first Workstation – Xerox Alto.

From: 1977 **UCLA**
To: 1982 Los Angeles, CA
Position: *Research Assistant & Senior Research Engineer, Computer Science Department*
Worked on VLSI Design and Testability, VLSI Design Methodology, Fault-Tolerant Computer Design and High Reliability, Computer Arithmetic and Design of Arithmetic Processor.

From: 1974 **University of Belgrade**
To: 1976 Belgrade, Yugoslavia
Position: *Assistant Professor, Electrical Engineering Department*
Research and teaching in Analog and Digital Electronics.

From: 1973 **Institute for Automation and Telecommunications**
To: 1974 Belgrade Yugoslavia
Position: *Research Engineer*
Design of non-standard analog circuitry for the analog part of the state of the art hybrid computer (project with USSR). Design of an Analog Multiplier based on Time Division Concept.

From: 1971 **Institute of Physics**
To: 1973 Belgrade Yugoslavia
Position: *Research Physicist*
Experimental work in plasma physics with extensive use of computer tools for simulation and data acquisition. Written software in Fortran on IBM 360/44 and CDC 6600.

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Consulting History Industry

From:	7/2016	**Esperanto Technologies, Inc.**
To:	4/2018	Mt View, California
	Duties:	processors
From:	10/2003	**Samsung Electronics Co. System LSI Division Research Laboratories**
To:	01/2004	Suwon-City, Gyeonggi-Do, Korea
	Duties:	Provided lectures on media processor architecture, clocking and clocked storage elements, power optimization of digital circuits.
From:	05/2002	**Intel Advanced Microprocessor Research Laboratories**
To:	09/2002	Hillsboro, OR
	Duties:	Developed Energy-Delay optimization methodology and tool for adders used in Itanium and P4 processors. Supervised two of my students in wireless 802.11 chip realization project.
From:	1997	**SONY, LSI Systems Laboratories**
To:	2001	San Jose, CA
	Duties:	Architect and project leader for new generation of media processors (reporting to the vice-president of SONY Corp.). Participated in strategic program planning as a member of the board.
From:	1996	**Hitachi Research and Development Laboratories**
To:	1999	San Jose, CA
	Duties:	Low-Power Design. Performed evaluation of clocked storage elements to be used in SH-5 processor. Work in low-power design.
From:	07/1994	**AT&T Bell Laboratories**
To:	09/1994	Holmdel, NJ
	Duties:	Development of new type of Low-Power circuits and logic based on energy-recovery principles.
From:	07/1992	**Sun Microsystems Laboratories**
To:	10/1992	Mountain View, CA
	Duties:	Worked on development of high-performance (1 GOP) super-scalar BiCMOS processor implementation and design.

Litigation Support Experience:

Date:	2021	**Winston & Strawn LLP** (lead attorney: Michael Rueckheim, James Lin)
	Case:	*Netlist, Inc. v. Micron Technology, Inc. et al.* (Case No. 6:21-cv-430 and -431), currently pending in the U.S. District Court for the Western District of Texas and conduct of inter partes review (IPR) proceedings before the U.S. Patent Office, Patent Trial and Appeal Board
	Parties:	Netlist, Inc. v. Micron Technology, Inc. et al.
	Project:	Netlist, Inc. v. Micron Technology, Inc. et al. (Case No. 6:21-cv-430 and -431), U.S. District Court for the Western District of Texas.
	Represent:	Micron Technology, Inc.
	Subject:	Consultation regarding patents, prior art, and other relevant aspects of the technology at issue in these Matters.
	Status:	Ongoing.
Date:	2021	**Dhillon Law Group Inc.** (attorney: Nitoj P. Singh)
	Case:	Cryplex Inc. v. Bitmain Technologies Holding Company, Superior Court of California – Santa Clara County, Case No. 18CV337836.
	Parties:	Cryplex Inc. v. Bitmain Technologies Holding Company.
	Project:	Identifying proprietary technology of Cryplex Inc.
	Represent:	Cryplex Inc.
	Subject:	Trade secret infringement project.
	Status:	Ongoing.
Date:	2021	**Cesari and McKenna, LLP**
	Case:	*WildlifeAcoustics, lnc. v. FrontierLabs PTY., Ltd,* l:20-cv-10620(GAO) (D. Mass.)
	Parties:	SRC LLC v. Intel Corp.
	Project:	Consulting services in connection with Frontier's litigation involving Wildlife Acoustics, Inc.
	Represent:	Frontier Labs PTY., Ltd.
	Subject:	Opinions and analysis relating to non-infringement of Frontier's accused products, including Expert Declaration.
	Status:	Ongoing.
Date:	2020	**Di Muro Ginsberg, P.C.**
	Case:	Case No. 3:17-cv-00561-WHO, United States District Court, Northern District of California.
	Parties:	SRC LLC v. Intel Corp.
	Project:	Expert in the Inter Partes Review dispute between SRC, and Intel Corp.
	Represent:	SRC LLC
	Subject:	Patent review.
	Status:	Closed.
Date:	2020	**Weeks Nelson LLP.**
	Case:	Red Hydrogen LLC v. CloudMinds (Hong Kong) Ltd. JAMS Arbitration No. 1220062943.
	Parties:	Red Hydrogen LLC v. CloudMinds (Hong Kong) Ltd.
	Project:	Expert opinion on manufacturing process of mobile phone.
	Represent:	Red Hydrogen LLC

	Subject:	Mobile phone manufacturing.
	Status:	Ongoing
Date:	2019	**Freitas & Weinberg LLP.**
	Case:	Aquila Innovations, Inc. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00554; Polaris Innovations Ltd. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00555 and Collabo Innovations, Inc. v. Advanced Micro Devices, Western District of Texas Case No. 1:18-cv-00552.
	Parties:	Aquila Innovations, Inc., Polaris Innovations Ltd. Collabo Innovations, Inc. v. Advanced Micro Devices.
	Project:	Three expert reports, rebuttal on expert report, tutorial to the Judge in the United States District Court, Western District of Texas, Austin Division, given on August 22, 2019.
	Represent:	Aquila Innovations, Inc, Polaris Innovations Ltd., Collabo Innovations, Inc.
	Subject:	Patent infringement.
	Status:	Unknown, presumed settled.
Date:	2019	**Antonelli, Harrington & Thompson LLP.**
	Case:	American Patents LLC v MediaTek et al. (6:18-cv-339) and American Patents LLC v. Analog Devices, Inc. et al. (6:18-cv-356). in The United States District Court for the Western District of Texas Waco Division.
	Parties:	*American Patents LLC. v. MediaTek et al.and Analog Devices, Inc.*
	Project:	Patent examination, claim construction, claim construction answering brief.
	Represent:	American Patents LLC
	Subject:	Patent infringement
	Status:	Unknown.
Date:	2018	**Morrison & Foerster LLP.**
	Case:	Case No. 3:17-cv-00561-WHO, United States District Court, Northern District of California.
	Parties:	*Synopsys, Inc. v. Ubiquiti Networks, Inc., et al.*
	Project:	Expert opinion on the Synopsys tool usage, *two expert reports*, *deposition testimony given, on August 31, 2018*.
	Represent:	Ubiquiti Networks, Inc..
	Subject:	Synopsys tool usage.
	Status:	Settled.
Date:	2017	**Swanson & Bratschun LLC.**
	Case:	Inter Parties Review Cases.
	Parties:	*Amazon.com, Inc. v. Avago Technologies General IP.*
	Project:	Reviewing patents, examining prior art, Inter Partes Review of various patents.
	Represent:	Avago Technologies.
	Subject:	Client – Server technology
	Status:	Settled.
Date:	2017	**Bunsow de Mory LLP.**
	Case:	Case Nos. 3:12-cv-03865, -03876, -03877, -03880, -03881 (N.D. Cal.)
	Parties:	*Technology Properties Limited LLC et al v. Huawei Technologies Co., Ltd.*
	Project:	Independent, *expert opinion on the patent*, claim construction, prior art.

Represent: Technology Properties Limited LLC et al.
Subject: Chip clocking
Status: Settled.

Date: 2016-2017 **Freitas Angell & Weinberg LLP**
Case: In the matter of Broadcom Corporation and Avago Technologies
Parties: *Broadcom and Avago vs Amazon*
Project: Patent examination, prior art examination,
Status: Settled 2017

Date: 2015-2106 **Desmarairs LLP.** (Attorney Sean T. Doyle)
Case: Civil Action No. 1:13-cv-00453-SLR
Parties: *Intellectual Ventures LLC vs. Toshiba Corp.*
Project: *Independent, expert opinion on the infringement*, patent, claim construction, invalidity contentions, writing expert report.
Represent: Intellectual Ventures LLC.
Subject: Processor on-chip testability, debugging and service.
Status: Settled.

Date: 2015-2106 **Farney Daniels PC**
Case: *Apple Inc., HTC Corp., HTC America Inc., Samsung Electronics Co. LTD and Samsung Electronics America Inc., Amazon.com Inc., v. Memory Integrity LLC*, USDC, Richmond, Virgina, Case: IPR2015-00163.
Parties: Apple Inc., HTC Corp., HTC America Inc., Samsung Electronics Co. LTD and Samsung Electronics America Inc., Amazon.com Inc., v. Memory Integrity LLC.
Project: Independent, *expert opinion on the litigation*, patent, *claim construction* etc. *Two deposistion testimonies: Nov. 24, 2015 and Jan. 8, 2016.*
Represent: Memory Integrity LLC., Patent Owner.
Subject: Cache coherency mechanism in multiprocessor system
Status: Settled 2016.

Date: 2015 **Latham and Watkins LLP**
Case: *Samsung Electronics Co. LTD and Samsung Electronics America Inc.*, *v. Nvidia Corp.,Old Micro Inc., F/K/A Velocity Micro Inc,.and Velocity Holdings, LLC,* USDC, Richmond, Virgina, CIVIL ACTION NO. 3:14-cv-00757-REP
Parties: Samsung Electronics Co. LTD and Samsung Electronics America Inc., Nvidia Corp. Old Micro Inc., F/K/A Velocity Micro Inc, and Velocity Holdings, LLC.
Project: Independent, *expert opinion on the litigation, patent, claim construction* etc. *Deposition testimony: October 29, 2015.*
Represent: Nvidia Corp., defendant.
Subject: Display power down technology
Status: Case settled

Date: 2015 **Nelson Bumgardner P.C.**
Case: *Technology Properties LTD. LLC, v. Barnes and Noble Inc. and Technology Properties LTD. LLC, Phoenix Digital Solutions LLC and Patriot Scientific Corp. vs. LG Electronics Inc. and LG Electronics USA Inc.*, USDC, N.D. Cal., Case No.: 3:12-CV-03863-VC, and Case No. 3:12-cv-03880-VC (PSG).

Parties: Technology Properties LTD. LLC, v. Barnes and Noble Inc. and Technology Properties LTD. LLC, Phoenix Digital Solutions LLC and Patriot Scientific Corp. vs. LG Electronics Inc. and LG Electronics USA Inc.
Project: Independent, *expert opinion on the patent, claim construction*, testifying services etc.
Represent: Technology Properties LTD. LLC.
Subject: Microprocessor clocking
Status: Case settled

Date: 2015 **Arnold and Porter LLP**
Case: *Synopsys Inc. v. Atop Tech Inc.*, USDC, N.D. Cal., Civil Case: No 3:13-cv-02965-MMC.
Parties: Synopsys Inc. v. Atop Tech Inc.
Project: *Independent, expert opinion on the patent*, testifying services etc.
Represent: Atop Tech Inc.
Subject: IC timing simulation, CAD.
Status: unknown

Date: 2015 **AZA Law**
Case: *Parthenon Unified Memory Architecture, v. HTC Corporation and HTC America Inc*, USDC, Eastern District of Texas, Marshal Division, Case No. 2:14-cv-00690
Parties: Parthenon Unified Memory Architecture, HTC Corporation and HTC America Inc.
Project: *Independent, expert opinion on the litigation*, patent, *claim construction* etc.
Represent: Parthenon Unified Memory Architecture, plaintiff.
Subject: Mobile phone chip shared memory function
Status: Settled

Date: 2012-14 **Otteson Law Group of Agility IP Law, LLP**
Case: *Acer, Inc., et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00877; *HTC Corporation, et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00882; *Barco NV v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-05398
Parties: Acer, Inc., Acer America Corporation, Gateway, Inc., Barco NV, Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited, HTC Corporation, HTC America, Inc.
Project: Patent infringement dispute related to computer circuits and logic. Study of patents and publications, *preparation of multiple expert reports*. (Transferred from Farella Braun + Martel LLP.)
Represent: Technology Properties Limited
Subject: Microprocessor clocking
Status: Settled, won
Work: ***Four deposition testimonies 2011, 2012, 2013***, Expert Report, Infringement Report, Two days testimony at International Trade Commission Court (June 5,6, 2013). Two weeks in the ITC court.

Court testimonies:

(a) ***International Trade Commission***, Washington, D.C., June 2013.

(b) ***Northern California District Court***, San Jose California. (I was the only expert on the side of TPL against half-dozen experts on the side of HTC). Three days of testimony, one week in court.
(c) Case won October 2, 2013.

Date: 2012 **Wolf Greenfield and Sacks P.C**
Case: *In the Matter of Certain Consumer Electronics and Display Devices and Products Containing Same*, USITC, Inv. No. 337-TA-836 and parallel district court actions *Graphics Properties Holdings, Inc. v. Research In Motion Ltd., et al.,* USDC, D. Del., Case No. CV11-01161 (and related actions CV11-01161, CV11-01162, CV11-01163, CV11-01164, CV11-01165)
Parties: Graphics Properties Holdings, Inc., Research In Motion Ltd., Research In Motion Corp., HTC Corporation, HTC America, Inc., LG Electronics, Inc., LG Electronics, LG Electronics MobileComm U.S.A., Apple Inc., Samsung Electronics Co., Ltd., Samsung Electronics Co. Ltd., Samsung Telecommunications, Sony Corporation, Sony Corporation of America, Sony Electronics, Inc., Sony Ericson Mobile, Sony Ericson Mobile
Project: *Preparing expert witness report*. Assisting in claim construction.
Represent: Graphics Properties Holdings, Inc.
Subject: Microprocessor clocking
Status: Settled: December 2012

Date: 2012 **Irell & Manella LLP**
Case: *Infineon Technologies AG, et al. v. Atmel Corporation*, USDC, D. Del., Case No. CV11-00307
Parties: Infineon Technologies AG, Infineon Technologies North America Corp., Atmel Corporation
Project: *Independent, expert opinion on the litigation, patent, claim construction* etc.
Represent: Atmel Corporation
Subject: Thermal and Power Management of Computer Systems
Status: Settled

Date: 2011 **Arnold and Porter LLP**
Case: *Optimum Power Solutions LLC vs. Hewlett-Packard Company*, USDC, N.D. Cal., Case No. CV12-03125 (transferred from USDC, D. Del., Case No. CV11-00853) (related cases in USDC, N.D. Cal., CV12-03127, CV12-03123, CV12-01509, CV12-03126; related cases in USDC, D.Del., CV11-00854, CV11-00855, CV11-00856)
Parties: Optimum Power Solutions LLC, Hewlett-Packard Company
Project: Patent infringement, search for prior art.
Represent: Hewlett-Packard Company
Subject: IC low-voltage operation, power management
Status: Closed

2009 **DLA Piper US LLP**
Case: *Zoran Corp vs. DTS Inc.*, Superior Court of California, County of Los Angeles, Northwest District, Case No. LC 083529
Parties: DTS Inc., Zoran Corp.

	Project:	Licensing / product infringement dispute. *Preparing expert witness report, expert testimony, expert rebuttal report*, product infringement investigation.
	Represent:	Zoran Inc.
	Subject:	DTS Algorithm, reverse engineering
	Status:	Settled
Date:	2008-11	**Farella Braun + Martel LLP**
	Case:	*Acer, Inc., et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00877; *HTC Corporation, et al. v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-00882; *Barco NV v. Technology Properties Limited, et al.*, USDC, N.D. Cal., Case No. CV08-05398
	Parties:	Acer, Inc., Acer America Corporation, Gateway, Inc., Barco NV, Technology Properties Limited, Patriot Scientific Corporation, Alliacense Limited, HTC Corporation, HTC America, Inc.
	Project:	Patent infringement case. *Preparing expert witness report*. Assisting in claim construction.
	Represent:	Technology Properties Limited
	Subject:	Microprocessor clocking, asynchronous communication, processor architecture
	Status:	Transferred to another attorney group
	Work:	*Two deposition testimonies given*, Claim construction, Patent invalidity analysis, Expert report, Prior art search.
Date:	2008-09	**Nixon Peabody LLP / Thelen LLP**
	Case:	*Technology Properties Limited, et al. v. HTC Corporation, et al.*, USDC, E.D. Tex., Case No. CV08-00174
	Parties:	Technology Properties Limited, Patriot Scientific Corporation, HTC Corporation, HTC America, Inc., Syrus XM, ASUSTeK Computer, Inc.
	Project:	Patent infringement case.
	Represent:	Technology Properties Limited
	Subject:	Microprocessor architecture, uP clocking
	Status:	Moved to another attorney firm, 2009, later won the case.
Date:	2008-09	**Townsend Townsend & Crew**
	Case:	TPL, case filed in Eastern District of Texas
	Parties:	TPL vs. Patriot Scientific Corporation, HTC Corporation, HTC America, Inc., Syrus XM, ASUSTeK Computer, Inc.
	Project:	Patent infringement case.
	Represent:	Technology Properties Limited
	Subject:	Computer circuits and logic, microprocessor asynchronous clocking
	Status:	Transferred to other law firms including Farella Braun + Martell, Nixon Peabody LLP / Thelen LLP.
	Work:	Patent invalidity prosecution assistance given, prior art search.
Date:	2007-08	**Dechert LLP**
	Case:	Acer, Inc., et al. v. Hewlett-Packard Company, USDC, W.D. Wisc., Case No. CV07-00620
	Parties:	Acer, Inc., Acer America Corporation, Hewlett-Packard Company
	Project:	Patent infringement dispute. *Preparing expert report*, product infringement investigation.

	Represent:	Hewlett-Packard Co.
	Subject:	Computer circuits and logic, microprocessor asynchronous clocking
	Status:	Closed
Date:	2007	**Townsend Townsend & Crew**
	Case:	*Technology Properties Limited Inc., et al. vs. Fujitsu Limited, et al.*, USDC, E.D. Tex., Case No. CV08-00494
	Parties:	Technology Properties Limited, Inc., Patriot Scientific Corporation, Fujitsu Limited, Fujitsu General America, Inc., Fujitsu Computer Products of America, Inc., Fujitsu Computer Systems Corp., Fujitsu Microelectronics America, Inc., Fujitsu Ten Corporation of America, Matsushita Electrical Industrial Co., Ltd., Panasonic Corporation of North America, JVC Americas Corporation, NEC Corporation NEC Electronics America, Inc., NEC America, Inc., NEC Display Solutions of America, Inc., NEC Solutions America, Inc., NEC Unified Solutions, Inc., Toshiba Corporation, Toshiba America, Inc., Toshiba America Electronics Components, Inc., Toshiba America Information Systems, Inc., Toshiba America Consumer Products, LLC, NEC Corporation of America, ARM Inc., ARM Ltd.
	Project:	Patent infringement dispute related to computer circuits and logic. Study of patents and publications, *preparation of expert reports*, assisting in a deposition.
	Represent:	Technology Properties Limited Inc.
	Subject:	Computer circuits and logic, microprocessor asynchronous clocking
	Status:	Closed
Date:	2004-06	**Kellogg, Huber Hansen Todd & Evans PLLC**
	Case:	OKI America, Inc. v. Advanced Micro Devices Inc., USDC, N.D. Cal., Case No. CV04-03171
	Parties:	OKI America, Inc., OKI Electric Industry Company, Ltd., OKI Data Corporation, OKI Data Americas, Inc., OKI Telecom, Inc., Advanced Micro Devices Inc., Pankaj Dixit,
	Project:	Preliminary patent invalidity contention. *Writing expert report*. *Deposition testimony*.
	Represent:	OKI plaintiffs
	Subject:	
	Status:	Closed
Date:	2005	**Irell & Manella LLP**
	Case	Examining Patent, No: 6,126,235. Contact attorney: Rudy Y. Kim
	Project:	Patent examination.
	Represent:	
	Subject:	
	Status:	Closed
Date:	2004	**Arent Fox Kintner Plotkin & Kahn, PLLC:**
	Case	*Hitachi Ltd.* Contact: Raymond J. Ho, Esq. Member (Partner)
	Project:	Product examination and chip analysis related to product infringement.
	Represent:	
	Subject:	
	Status:	Closed

Consultant Curriculum Vitae

Date:	2001	**Morgan Lewis & Bockius LLP**
	Case:	unknown
	Project:	Patent examination.
	Represent:	
	Subject:	
	Status:	Closed
Date:	1999-00	**Townsend Townsend & Crew**
	Case	*Sun Microsystems v. IBM.*
	Parties:	Sun Microsystem, IBM Corp.
	Project:	Patent infringement dispute related to computer circuits and logic: Study of patents and publications, preparation of expert report.
	Represent:	Sun Microsystem
	Subject:	Computer circuits and logic
	Status:	Case successfully settled
Date:	1998	**Weil Gotshal & Manges LLP**
	Case:	unknown
	Parties:	
	Project:	Patent examination. Two patents examined.
	Represent:	
	Subject:	
	Status:	Closed
Date:	1997-98	**Bernstein Litowitz Berger & Grossmann LLP**
	Case:	Edward McDaid, et al., On Behalf Of Themselves and All Others Similarly Situated v. Walter J. Sanders, III, et al., USDC, N.D. Cal., Case No. CV95-20750
	Parties:	Edward McDaid, et al., On Behalf Of Themselves and All Others Similarly Situated, Walter Jeremiah Sanders, III, Anthony B. Holbrook, Richard Previte, Marvin D. Burkett, Advanced Micro Devices, Inc.
	Project:	Class action case, analysis of AMD K5 processor design, *writing expert report* and participating in deposition as an assisting expert to the attorney.
	Represent:	Edward McDaid, et al.
	Subject:	Microprocessor design, AMD K5, schedule, debug, project management
	Status:	Case successfully settled (award amount $15 million)

U.S. Patents: Vojin G. Oklobdzija

Patent Number	Date Issued	Title
20230087096-A1	3/23/2023	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE AND TEMPERATURE (PVT) VARIATIONS
20230045265-A1	2/09/2023	FAST CLOCKED STORAGE ELEMENT
20230015430-A1	1/19/2023	FLOATING-POINT ACCUMULATOR
11,558,041 B1	1/17/2023	FAST CLOCKED STORAGE ELEMENT
20230004353-A1	1/5/2023	FLOATING POINT ACCUMULATER WITH A SINGLE LAYER OF SHIFTERS IN THE SIGNIFICAND FEEDBACK
20220308834-A1	9/29/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
11442696-B1	9/13/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
11,429,349 B1	8/30/2022	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH CARRY-SAVE ACCUMULATOR
11411553-B1	8/9/2022	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE AND TEMPERATURE (PVT) VARIATIONS
11366638	06/21/2022	FLOATING POINT MULTIPLY – ADD, ACCUMULATE UNIT WITH COMBINED ALIGNMENT CIRCUITS
11,442,696	11/23/2021	FLOATING POINT MULTIPLY-ADD, ACCUMULATE UNIT WITH EXCEPTION PROCESSING
10,707,839	07/07/2020	SYSTEM OF FREE RUNNING OSCILLATORS FOR DIGITAL SYSTEM CLOCKING IMMUNE TO PROCESS, VOLTAGE, AND TEMPERATURE (PVT) VARIATIONS
7,509,486	03/24/2009	ENCRYPTION PROCESSOR FOR PERFORMING ACCELERATED COMPUTATIONS TO ESTABLISH SECURE NETWORK SESSIONS CONNECTIONS
6,753,715	06/22/2004	SYSTEM FOR SYMMETRIC PULSE GENERATOR FLIP-FLOP
20040057313-A1	3/25/2004	SYSTEM FOR SYMMETRIC PULSE GENERATOR FLIP-FLOP
6,693,459	02/17/2004	METHOD AND SYSTEM FOR IMPROVING SPEED IN A FLIP-FLOP,"
6,647,487	11/11/2003	METHOD AND SYSTEM FOR REDUCING HAZARDS IN A FLIP-FLOP
6553541-B1	4/22/2003	REDUCED-COMPLEXITY SEQUENCE DETECTION
20030062940-A1	4/3/2003	METHOD AND SYSTEM FOR REDUCING HAZARDS IN A FLIP-FLOP
20030062925-A1	4/3/2003	METHOD AND SYSTEM FOR IMPROVING SPEED IN A FLIP-FLOP
20030056129-A1	3/20/2003	CONDITIONAL PRE-CHARGE METHOD AND SYSTEM
20020143841-A1	3/10/2002	MULTIPLEXER BASED PARALLEL N-BIT ADDER CIRCUIT FOR HIGH SPEED PROCESSING
6,353,843	03/05/2002	HIGH PERFORMANCE UNIVERSAL MULTIPLIER

6,301,599	10/09/2001	MULTIPLIER CIRCUIT HAVING OPTIMIZED BOOTH ENCODER/SELECTOR
6,282,556	08/28/2001	HIGH PERFORMANCE PIPELINED DATA PATH FOR A MEDIA PROCESSOR
6,243,728	06/05/2001	PARTITIONED SHIFT RIGHT LOGIC WITH ROUNDING SUPPORT
6,232,810	05/15/2001	FLIP-FLOP
6,128,641	10/03/2000	DATA PROCESSING UNIT WITH HARDWARE ASSISTED CONTEXT SWITCHING CAPABILITY
4,992,398	02/12/1991	INSTRUCTION CONTROL MECHANISM FOR A COMPUTING SYSTEM WITH REGISTER RENAMING AND QUEUES INDICATING AVAILABLE REGISTERS
4,847,759	07/11/1989	REGISTER SELECTION MECHANISM AND ORGANIZATION OF AN INSTRUCTION PREFETCH BUFFER
4,714,994	12/22/1987	INSTRUCTION PREFETCH BUFFER CONTROL
4,700,086	10/13/1987	CONSISTENT PRECHARGE CIRCUIT FOR CASCODE VOLTAGE SWITCH LOGIC

European Patents: Vojin G. Oklobdzija

EP1058394 **European Patent:** NIKOLIC BORIVOJE (US); FU LEO (US); LEUNG MICHAEL (US); OKLOBDZIJA VOJIN G (US); YAMASAKI RICHARD (US), Reduced complexity sequence detection (US19990129149P 19990414)

EP1012715 **European Patent:** R. Fleck, R. Arnold, B. Holmer, V.G. Oklobdzija, Eric Chesters, "DATA PROCESSING UNIT WITH HARDWARE ASSISTED CONTEXT SWITCHING CAPABILITY," European Patent Issued, June 28, 2000.

EP0195202 **European Patent:** OKLOBDZIJA VOJIN G; "Register selection mechanism and organization of an instruction prefetch buffer"; Publication date: 1986-09-24. **Applicant:** IBM (US)

EP0297265 **European Patent:** COCKE JOHN; GROHOSKI GREGORY FREDERICK; OKLOBDZIJA VOJIN G; "An instruction control mechanism for a computer system" **Publication date:** 1989-01-04. **Applicant:** IBM (US).

EP0199946 **European Patent:** OKLOBDZIJA VOJIN G; LING DANIEL T; "Instruction prefetch buffer control and method of controlling an instruction prefetch buffer," **Publication date:** 1986-11-05; **Applicant:** IBM (US)

EP0206462 **European Patent:** LING DANIEL TAJEN; OKLOBDZIJA VOJIN G; RAVER NORMAN; "Method of precharging and precharge circuit for dynamic cascode voltage switch logic"; **Publication date:** 1986-12-30; **Applicant:** IBM (US)

Japanese Patents: Vojin G. Oklobdzija

JP2001053622 **Japan Patent**: LEUNG MICHAEL; FU LEO; NIKOLIC BORIVOJE; OKLOBDZIJA VOJIN G; YAMASAKI RICHARD, "METHOD FOR SIMPLIFIED VITERBI DETECTION FOR SEQUENCE DETECTION AND VITERBI DETECTOR," Issued: February 23, 2001.

JP1017126 **Japan Patent**: COCKE JOHN; GROHOSKI GREGORY FREDERICK; OKLOBDZIJA VOJIN G, "REGISTER RENAMING DEVICE," Issued: January 20, 1989.

JP61214029 **Japan Patent**: OKLOBDZIJA VOJIN G; "Register selection mechanism and organization of an instruction prefetch buffer"; Issue date: **Applicant:** IBM (US).

JP1017126 **Japan Patent**: COCKE JOHN; GROHOSKI GREGORY FREDERICK; OKLOBDZIJA VOJIN G; "An instruction control mechanism for a computer system" **Issue date:** 1989-01-04. **Applicant:** IBM (US).

JP61256446 **Japan Patent**: OKLOBDZIJA VOJIN G; LING DANIEL T; "Instruction prefetch buffer control and method of controlling an instruction prefetch buffer," **Issue date: Applicant:** IBM (US)

JP61247122 **Japan Patent**: LING DANIEL TAJEN; OKLOBDZIJA VOJIN G; RAVER NORMAN; "Method of precharging and precharge circuit for dynamic cascode voltage switch logic"; **Issue date:**; **Applicant:** IBM (US).

PATENTS: World Intellectual Property Organization patents

WO0127742 **WIPO patent**: CHEHRAZI FARZAD; OKLOBDZIJA VOJIN G; FAROOQUI AAMIR A, "A PARTITIONED MULTIPLIER"; **Publication date:** 2001-04-19. **Applicant:** SONY ELECTRONICS INC (US).

WO0104724 **WIPO patent:** OKLOBDZIJA VOJIN; CHEHRAZI FARZAD; LI WEI-JEN; YU ANDY W, FAROOQUI AAMIR; "A PARTITIONED RIGHT SHIFT LOGIC CIRCUIT HAVING ROUNDING SUPPORT"; **Publication date:** 2001-01-18. **Applicant:** SONY ELECTRONICS INC (US).

WO0057270 **WIPO patent**: FAROOQUI AAMIR A; OKLOBDZIJA VOJIN G; CHEHRAZI FARZAD; "ADDER CIRCUIT"; **Publication date:** 2000-09-28. **Applicant:** SONY ELECTRONICS INC (US).

WO0059112 **WIPO patent**: CHEHRAZI FARZAD; OKLOBDZIJA VOJIN G; FAROOQUI AAMIR A; "MULTIPLIER CIRCUIT"; **Publication date:** 2000-10-05. **Applicant:** SONY ELECTRONICS INC (US).

WO0140934 **WIPO patent**: CHEHRAZI FARZAD; OKLOBDZIJA VOJIN G; "PIPELINED DATA PATH CIRCUIT"; **Publication date:** 2001-06-07. **Applicant:** SONY ELECTRONICS INC (US).

WO9914671 **WIPO patent**: FLECK ROD G; ARNOLD ROGER D; HOLMER BRUCE; OKLOBDZIJA VOJIN; CHESTERS ERIC; "DATA PROCESSING UNIT WITH HARDWARE ASSISTED CONTEXT SWITCHING CAPABILITY"; **Publication date:** 1999-03-25 **Applicant:** INFINEON TECHNOLOGIES NORTH AMERICA CORP.

PUBLICATIONS (Vojin G. Oklobdzija)

(Citations h-index = 46[4] ; 8,238 citations in Google Scholar; i10 index = 112)

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[1] V. G. Oklobdzija, *"High-Performance System Design: Circuits and Logic,"* IEEE Press, July, 1999.

[2] V. G. Oklobdzija, *"Computer Engineering,"* CRC Press, December 2001. (Selected as "Outstanding Academic Title" in 2002 by Choice Magazine out of 22,000 titles).

[3] V. G. Oklobdzija et al, "Digital System Clocking: High-Performance and Low-Power Aspects," John Wiley Publishing, January 2003.

[4] V. G. Oklobdzija, R. K. Krishnamurthy, *"High Performance Energy Efficient Microprocessor Design,"* Springer, ISBN: 0-387-28594-6, June 2006.

[5] V. G. Oklobdzija, *"Digital Systems and Applications,"* Taylor & Francis Publishing, December 2007.

[6] V. G. Oklobdzija, *"Digital Design and Fabrication,"* Taylor & Francis Publishing, December 2007.

Books Published under my editorship in Computer Engineering book series:

[7] C. Piguet, "Low-Power Electronics Design," CRC Press, August, 2004.

[8] B. Vasic, E. M. Kurtas, "Coding and Signal Processing for Magnetic Recording Systems," CRC Press, November 2004.

[9] T. Reed, "Digital Image Sequence Processing, Compression and Analysis," CRC Press, 2004.

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[1] V. G. Oklobdzija, "Computer Arithmetic," The Electrical Engineering Handbook, R. C. Dorf (Ed.), a Chapter, CRC Press, Inc., pp. 1858-1865, 1993.

[2] V. G. Oklobdzija, "Computer Organization: Architecture," *The Engineering Handbook*, R. C. Dorf (Ed.), a Chapter, CRC Press, Inc., 1995.

[3] V. G. Oklobdzija, "Digital Systems" , *The Engineering Handbook*, R. C. Dorf (Ed.), Introduction into Digital Systems, Chapter, CRC Press, Inc., 1995.

[4] V. G. Oklobdzija, "Computers" , *The Engineering Handbook*, R. C. Dorf (Ed.), Introduction into Computers, a Chapter, CRC Press, Inc., 1995.

[4] **Wikipedia**: 45 or higher (h-index) could mean membership in the United States National Academy of Sciences. Hirsch estimated that after 20 years a "successful scientist" would have an *h*-index of 20, an "outstanding scientist" would have an *h*-index of 40, and a "truly unique" individual would have an *h*-index of 60.

[5] V. G. Oklobdzija, *"Digital Arithmetic,"* Wiley Encyclopedia of Electrical and Electronics Engineering, Book Chapter, John Wiley publishing, 1999.

[6] V. G. Oklobdzija, *"Reduced Instruction Set Computing,"* Vol.18, Wiley Encyclopedia of Electrical and Electronics Engineering, Book Chapter, John Wiley publishing, 1999.

[7] V. Oklobdzija, *"High-Speed VLSI Arithmetic Units: Adders and Multipliers,"* in "Design of High-Performance Microprocessor Circuits," Book Chapter, Book edited by A. Chandrakasan, IEEE Press, 2000.

[8] V. G. Oklobdzija, "Clocking Multi-GHz Systems," *Low-Power Electronics Design*, C. Piguet (Ed.), a Chapter, CRC Press, Inc., 2004.

[9] N. M. Nedovic, V. G. Oklobdzija, "Clocked Storage Elements in Digital Systems", in *"High Performance Energy Efficient Microprocessor Design"* V.G. Oklobdzija, R.K. Krishnamurthy (Ed.), a Chapter, Springer, 2006.

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[11] V. G. Oklobdzija, B.R. Zeydel, "Energy-Delay Charachteristics of CMOS Adders", in *"High Performance Energy Efficient Microprocessor Design"* V.G. Oklobdzija, R.K. Krishnamurthy (Ed.), a Chapter, Springer, 2006.

JOURNAL PAPERS:

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[2] V. G. Oklobdzija, "Up/Down Display Counter Counts Over Pos/Neg Range," *Digital Design*, pp. 94-95, 1981.

[3] V. G. Oklobdzija and M. D. Ercegovac, "An On-Line Square Root Algorithm," *IEEE Transactions on Computers*, Vol. C-31, No. 1, pp. 70-75, 1982.

[4] V. G. Oklobdzija, "Design Note. Opto-Isolated RS-232 Interface Achieves High Data Rate," Electronics, Vol. 55, No. 1, p. 175, 1982.

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[7] V. G. Oklobdzija and E. R. Barnes, "On Implementing Addition In VLSI Technology," *IEEE Journal of Parallel and Distributed Computing*, No. 5, pp. 716-728, 1988.

[8] B. D. Lee and V. G. Oklobdzija, "Improved CLA Scheme with Optimized Delay," *Journal of VLSI Signal Processing*, Vol. 3, No. 4, pp. 265-274, 1991.

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[10] V. G. Oklobdzija, "Algorithmic Design of A Hierarchical And Modular Leading Zero Detector Circuit," *Electronics Letters*, Vol. 29, No. 3, pp. 283-284, 1992.

[11] V. G. Oklobdzija, D. Villeger, and T. Soulas, "An Integrated Multiplier For Complex Numbers," *Journal of VLSI Signal Processing*, Vol. 7, No. 3, pp. 213-222, 1993.

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[16] M. N. Dorojevets and V. G. Oklobdzija, "Multithreaded Decoupled Architecture," *International Journal of High-Speed Computing*, World Scientific Publisher, 18 pages, June, 1995.

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[123] V.G. Oklobdzija, M. Aktan, Baran, "*Optimal Transistor Sizing and Voltage Scaling for Minimal Energy use at Fixed Performance*", 7th Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA 2012), Cordoba, Argentina, August 4-12, 2012.

[124] V. Nawathe, M. Aktan, L. Wang, V. G. Oklobdzija, "*Parallelism trade-offs for data-driven circuits*", 7th Argentine School of Micro-Nanoelectronics, Technology and Applications (EAMTA 2012), Cordoba, Argentina, August 4-12, 2012.

[125] M. Aktan, D. Baran, V.G. Oklobdzija, "*Minimizing Energy by Achieving Optimal Sparseness in Parallel Adders*", 22nd IEEE Symposium on Computer Arithmetic, Lyon, FRANCE, June 22-24, 2015.

PRESENTATIONS: Vojin G. Oklobdzija

1. 1982 VLSI TECHNOLOGY. Electrical Engineering Department, University of Belgrade, Yugoslavia, September 18, 1982.

2. 1982 TESTABILITY ENHANCEMENT OF VLSI USING CIRCUIT STRUCTURES. Presented at the ICCC '81 IEEE International Conference on Circuits and Computers, New York, NY, September 28 - October 1, 1982.

3. 1983 IMPROVING TESTABILITY BY USING ADDITIONAL CIRCUITS. Presented at the Seventeenth Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, October 31 - November 2, 1983.

4. 1984 ON TESTABILITY OF CVS LOGIC. Presented at IBM Internal Technical Liaison Symposium, La Grande, France, April 3-5, 1989.

5. 1984 TEST GENERATION FOR FET SWITCHING CIRCUITS. Presented at the Internal Test Conference, Philadelphia, PA, October 16-18, 1984.

6. 1984 ON TESTABILITY OF CMOS-DOMINO LOGIC. Presented at the 14th International Symposium on Fault Tolerant Computing, Orlando, FL, June 20-22, 1984.

7. 1985 SOME OPTIMAL SCHEMES FOR ALU IMPLEMENTATION IN VLSI TECHNOLOGY. Presented at the 7th Symposium on Computer Arithmetic, Urbana, IL.

8. 1985 DESIGN-PERFORMANCE TRADE-OFFS IN CMOS-DOMINO LOGIC. Presented at the Custom Integrated Circuits Conference, Portland, Or, May 22, 1985.

9. 1986 ALGORITHM FOR IMPLEMENTATION OF A FAST AND OPTIMAL ALU IN VLSI TECHNOLOGY. Computer Science Department, University of California at Los Angeles, Los Angeles, California, February 18, 1986.

10. 1986 DESIGN TRADE-OFFS IN VLSI TECHNOLOGY. Electrical Engineering Department, Columbia University, New York, N.Y., March 7, 1986.

11. 1986 TESTABILITY OF DYNAMIC CMOS CIRCUITS. Fifth IEEE West Coast Workshop, Lake Tahoe, California, April 20-23, 1986.

12. 1986 REDUCED INSTRUCTION SET ARCHITECTURES FOR VLSI IMPLEMENTATION. Electrical Engineering Department, University of Belgrade, Yugoslavia, September 9, 1986.

13. 1987 SINGLE-CHIP ARCHITECTURE FOR REAL-TIME COMPUTATION OF THE WIGNER DISTRIBUTION OF ACOUSTIC SIGNALS. Presented at the 21st Asilomar Conference on Signals, Systems, and Computers, November 2-4, Pacific Grove.

14. 1988 ARCHITECTURAL STUDY OF AN INTEGRATED FIXED AND FLOATING-POINT VLSI-ASIC PROCESSOR. University of California Irvine, Irvine, California, March 23, 1988.

15. 1988 EFFICIENT VLSI ALGORITHM FOR FAST ALU IMPLEMENTATION. Department of Computer Engineering, University of California, Santa Cruz, November 17, 1988.

16. 1988 ARCHITECTURE FOR SINGLE-CHIP ASIC PROCESSOR WITH INTEGRATED FLOATING-POINT UNIT. Presented at the 21st Hawaii International Conference on System Sciences, Kailua-Kona, Hawaii, January 5-7, 1988.

17. 1988 ARCHITECTURAL STUDY FOR AN INTEGRATED FIXED AND FLOATINGPOINT VLSI-ASIC PROCESSOR. Presented at COMPEURO-'88. Symposium on Circuits and Systems, Brussels, April 11-14, 1988.

18. 1989 EFFICIENT VLSI IMPLEMENTATION OF ADDITION. University of San Diego, San Diego, California, February 23, 1989.

19. 1989 801: A PERSPECTIVE ON IBM RISC. Electrical Engineering Department, Stanford University, California, April 19, 1989.

20. 1989 PERSPECTIVE ON RISC ARCHITECTURE. Monterey Institute of Technology, Queretaro, Mexico, July 10, 1989.

21. 1989 RECENT DEVELOPMENTS IN VLSI TECHNOLOGY, CONCITEQ. Technology Institute of the State of Queretaro, Queretaro, Mexico, July 17, 1989.

22. 1989 STUDY OF FAST ADDER IMPLEMENTATIONS. Electrical Engineering Department Seminar, Stanford University, California, December 13, 1989.

23. 1991 EVOLUTION OF RISC INTO SUPER-SCALAR ARCHITECTURE AND A LOOK BEYOND. Computer Sciences Department Seminar, Columbia University, February 20, 1991.

24. 1991 ISSUES IN RISC AND SUPER-SCALAR ARCHITECTURE. Electrical Engineering Department Seminar, Princeton University, April 16, 1991.

25. 1991 SUPER-SCALAR ARCHITECTURE AND BEYOND. NEC Corporate Research Center Seminar, Princeton New Jersey, April 17, 1991.

26. 1991 ADVANCES IN CONTEMPORARY RISC ARCHITECTURE. 1991 Belgrade Summer School on Modern Computer Architecture, Short Course, Sava Congress Center, May 8-9, 1991.

27. 1991 PERSPECTIVE ON SIMD ARCHITECTURES AND APPLICATIONS. Advanced Computer Research Institute Seminar, ACRI Lyon FRANCE, May 14, 1991.

28. 1991 PROGRAMAS PARA ENSENAR COMPUTACION EN UNIVERSIDADES. Short Course (in Spanish), Asemblea de Rectores, Lima PERU, sponsored by Fulbright program, September 10-13, 1991.

29. 1991 TEMAS AVANZADAS DE LA ARQUITECTURA DE COMPUTADORES. Short Course (in Spanish), Asemblea de Rectores, Lima PERU, sponsored by Fulbright program, September 16-19, 1991.

30. 1991 REDES DE COMPUTADORAS. Short Course (in Spanish), Asemblea de Rectores, Lima PERU, sponsored by Fulbright program, September 23-26, 1991.

31. 1991 PLANO POR DESARROLLO DE REDES LOCALES EN UNIVESIDADES. Seminar (in Spanish), Universidad Nacional de Ingenieria, Lima PERU, sponsored by Fulbright program, September 18, 1991.

32. 1991 PLANIFICACION Y DESARROLLO DE COMPUTATORAS EN UN AMBIENTE ACADEMICO. Seminar (in Spanish), Pontifica Universidad Catolica del Peru, Lima PERU, sponsored by Fulbright program, September 25, 1991.

33. 1991 PERSPECTIVAS POR DESARROLLO DE COMPUTACION EN UN PAIS DE TERCER MUNDO. Seminar (in Spanish), Universidad Mayor de San Marcos (the oldest university of Americas), Lima, PERU, September 26, 1991.

34. 1992 ISSUES IN SUPER-SCALAR ARCHITECTURE: Pipelining and Contention Resolution, Invited Talk, Centre for Signal Processing Research, Space Centre for Satelite Navigation, Queensland University of Technology, Brisbane, Australia, May 18th, 1992.

35. 1992 SIMD MACHINES: IBM's GF-11, Seminar, Department of Electronic Engineering, La Trobe University, Melbourne, Australia, May 25, 1992.

36. 1992 RECONFIGURABLE PROCESSOR FOR REAL-TIME SIGNAL ANALYSIS, Seminar, Department of Electronic Engineering, La Trobe University, Melbourne, Australia, May 26, 1992.

37. 1992 PRINCIPLES OF RISC ARCHITECTURE AND THEIR INFLUENCE ON SUPERSCALARS: A RISC PERSPECTIVE, Invited Talk, Melbourne University, Greenwood Lecture Theatre, Melbourne, Australia, May 27, 1992.

38. 1992 ISSUES IN SUPER-SCALAR ARCHITECTURE: PIPELINING AND CONTENTION RESOLUTION, Invited Talk, CITRI - Commonwealth Information Technology Research Institute, Melbourne, Australia, May 27, 1992.

39. 1992 ISSUES IN OPTIMIZING CACHE HIERARCHY FOR PERFORMANCE, Seminar, Department of Electronic Engineering, La Trobe University, Melbourne, Australia, May 28, 1992.

40. 1992 PRINCIPLES OF RISC ARCHITECTURE AND THEIR INFLUENCE ON SUPERSCALARS, Seminar, Department of Computer Sciences, University of Waikato, Hamilton, New Zealand, June 4, 1992.

41. 1992 RESEARCH DIRECTIONS IN COMPUTER ENGINEERING, Seminar, Intel Corporation, Folsom, California, October 14, 1992.

42. 1993 DEVELOPMENT OF COMPUTER ARITHMETIC ALGORITHMS AND MAPPING OF ALGORITHMS INTO TECHNOLOGY, Seminar, LSI Logic Corporation, Milpitas, California, January 22, 1993.

43. 1993 EVOLUTION OF RISC INTO SUPER-SCALAR ARCHITECTURE: PERSPECTIVE ON RISC, IEEE Seminar at San Francisco State University, San Francisco, California, March 11, 1993.

44. 1993 MULTIPLIER DESIGN UTILIZING IMPROVED COLUMN COMPRESSION TREE AND OPTIMIZED FINAL ADDER IN CMOS TECHNOLOGY, 10th Anniversary 1993 International Symposium on VLSI Technology, Systems and Applications, Taipei, TAIWAN, May 12-14, 1993.

45. 1993 MULTIPLIER OPTIMIZATION IN CMOS TECHNOLOGY, Seminar, Toshiba ULSI Technology Center, Toshiba Corporation, Kawasaki, JAPAN, May 17, 1993.

46. 1993 ISSUES IN SUPER-SCALAR ARCHITECTURE: PIPELINING AND CONTENTION RESOLUTION, Seminar, Department of Information Sciences, Kyoto University, Kyoto, JAPAN, May 20, 1993.

47. 1993 MULTIPLIER SPEED OPTIMIZATION: IMPROVED COLUMN COMPRESSION ALGORITHM AND OPTIMIZATION OF THE FINAL ADDER, Seminar, Hitachi Ltd. Central Research Laboratory, Tokyo, JAPAN, May 21, 1993.

48. 1993 MULTIPLIER DESIGN CONSIDERATIONS IN CMOS: USE OF IMPROVED COLUMN COMPRESSION TREE AND OPTIMIZED FINAL ADDER, Seminar, LSI Logic Corporation, Milpitas, California, June 16, 1993.

49. 1993 HIGH-PERFORMANCE PROCESSOR DESIGN ISSUES: PIPELINE SELECTION AND MATCHING OF THE INSTRUCTION SET, Seminar, Hitachi America Ltd., Brisbane, California, June 25, 1993.

50. 1993 DESIGNING A PARALLEL MULTIPLIER OPTIMIZED FOR SPEED, UCLA Computer Science Seminar, Department of Computer Sciences, UCLA, Los Angeles, California, July 23, 1993.

51. 1993 HIGH-PERFORMANCE COMPUTER ARCHITECTURE: SUPER-SCALAR AND RISC, National University of Singapore, Department of Computer Science, September 15, 1993.

52. 1993 A HIERARCHICAL AND MODULAR CIRCUIT IMPLEMENTING LEADING ZERO DETECTOR FOR A HIGH-PERFORMANCE FLOATING-POINT PROCESSOR, 5th International Symposium on IC Technology, Systems and Applications, ISIC-93, Nanyang Technological University, Singapore, September 16.

53. 1993 RISC AND HIGH-PERFORMANCE SINGLE PROCESSOR ARCHITECTURES, Computer Science Seminar, University of Sains, Pulau-Pinang, Malaysia, September 21, 1993.

54. 1993 DIRECTIONS IN PARALLEL COMPUTER ARCHITECTURES, Computer Science Seminar, University of Sains, Pulau-Pinang, Malaysia, Septermber 23, 1993.

55. 1993 CONTENTION RESOLUTION AND PIPELINE ISSUES IN SUPER-SCALAR ARCHITECTURES: IBM RS/6000, Computer Architecture Seminar, University of California, Davis, California, November 11.

56. 1993 PRINCIPLES OF RISC ARCHITECTURE AND ITS EVOLUTION INTO SUPERSCALARS: A RISC PERSPECTIVE, UNINET Video Conference Seminar, The University of Sydney, University of New South Wales, Monash University, University of Technology Sydney, Sydney, AUSTRALIA, December 14, 1993.

57. 1993 SUPER-SCALAR ARCHITECUTURE ISSUES: INSTRUCTION PHILOSOPHY AND CONTENTION RESOLUTION IN THE IBM RS/6000, UNINET Video Conference Seminar, The University of Sydney, University of New South Wales, Monash University, University of Technology Sydney, Sydney, AUSTRALIA, December 16, 1993.

58. 1994 TECHNOLOGY UNDER CONTROL: ETHICS AND RESPONSIBILITY OF AN ENGINEER, Society of Women in Engineering, School of Engineering, University of California, Davis, California, February 2, 1994.

59. 1994 DEVELOPMENT OF RISC ARCHITECTURE: AN INSIDER'S UNORTHODOX PERSPECTIVE, IEEE Seminar, School of Engineering, University of California, Davis, California, February 23, 1994.

60. 1994 A METHOD FOR GENERATION OF FAST PARALLEL MULTIPLIERS, Computer Engineering Seminar, Department of Electrical Engineering, University of California, Davis, California, May 17, 1994.

61. 1994 A METHOD FOR GENERATION OF FAST PARALLEL MULTIPLIERS, Seminar, Research and Development Department, Hitachi America Ltd., Brisbane, California, May 27, 1994.

62. 1994 ON TESTABILITY OF PASS-TRANSISTOR LOGIC, Seminar, Research and Development Department, Hitachi America Ltd., Brisbane, California, May 27, 1994.

63. 1994 AN ECL GATE FOR HIGH-SPEED AND LOW-POWER LOGIC IN BICOMOS PROCESS. Presented at the High-Speed Electronics Research Department, AT&T Bell Laboratories, Holmdel, New Jersey, July 21st, 1994.

64. 1994 ADIABATIC CIRCUITS FOR LOW POWER COMPUTATION. Electrical Engineering Department, Imperial College, London, England, July 26th, 1994.

65. 1994 ADIABATIC LOGIC AND LOW ENERGY COMPUTATION. Seminar at NEC USA C&C Research Laboratories, Princeton, New Jersey, August 10, 1994.

66. 1994 USE OF ADIABATIC LOGIC FOR LOW ENERGY COMPUTATION. Seminar. Department of Electrical Engineering, Princeton University, August 10, 1994.

67. 1994 PROGRESS IN DEVELOPMENT OF ADIABATIC CIRCUITS AND LOGIC. Seminar, VLSI Research Department, AT&T Bell Laboratories, August 19, 1994.

68. 1994 THE OUTLOOK FOR DEVELOPMENT OF COMPUTING AND DIGITAL SYSTEMS IN THE NEXT DECADE. Invited Distinguished Lecture, Department of Electrical Engineering, University of Belgrade, Yugoslavia, September 26, 1994.

69. 1994 LOGIC SYNTHESIS FOR ASIC. Invited Lecture, Institute of Automation, Chinese Academy of Science, Beijing, P. R. of China, October 18, 1994.

70. 1994 DEVELOPMENT AND SYNTHESIS OF DUAL VALVE LOGIC USING PASS TRANSISTOR DESIGN TECHNIQUE. Invited Lecture, Institute of Microelectronics, Chinese Academy of Science, Beijing, P. R. of China, October 18, 1994.

71. 1994 LOGIC SYNTHESIS USING GUIDED ALGORITHMIC APPROACH. Invited Lecture, Department of Electrical Engineering, Tsinghua University, Beijing, P. R. of China, October 19, 1994.

72. 1994 LOGIC SYNTHESIS FOR ASIC: A GUIDED ALGORITHMIC APPROACH. First International Conference on ASIC, Fragrant Hill, Beijing, P. R. of China, October 20, 1994.

73. 1994 SYSTEM FOR RAPID PROTOTYPING OF APPLICATION SPECIFIC SIGNAL PROCESSORS FOR ASIC IMPLEMENTATION. First International Conference of ASIC, Fragrant Hill, Beijing, P. R. of China, October 20, 1994.

74. 1994 A METHOD FOR GENERATION OF SPEED OPTIMIZED PARALLEL MULTIPLIER. Special Seminar, Hitachi Central Research Laboratory, Kokubunji, Tokyo, JAPAN, October 24, 1994.

75. 1995 PERFORMANCE ISSUES IN SUPER-SCALAR RISC PROCESSORS: VALUE OF REGISTER RENAMING ALGORITHM, Seminar at San Francisco State University, San Francisco, California, March 11, 1995.

76. 1995 RE-ENGINERIA DE SISTEMAS DE INFORMACION PARA LOS ANOS 90, 1st International Conference on System Engineering, Lima, PERU, June 1st, 1995 (in Spanish).

77. 1995 SISTEMAS DE INFORMACION: ARQUITECTURA DE SISTEMAS MODERNOS, 1st International Conference on System Engineering, Lima, PERU, June 1-2, 1995 (two-day workshop in Spanish).

78. 1995 OPTIMAL STRATEGIES FOR PARALLEL MULTIPLIER DESIGN, Electrical Engineering Department, University of Belgrade, Yugoslavia, July 28, 1995.

79. 1995 NEW DIFFERENTIAL LOGIC BASED ON PASS-TRANSISTOR DESIGN, Electrical Engineering Department, University of Belgrade, Yugoslavia, September 14, 1995.

80. 1995 ALGORITHM AND METHOD FOR SYNTHESIS OF FAST PARALLEL MULTIPLIER, Electrical Engineering Department, University of Belgrade, Yugoslavia, September 15, 1995.

81. 1995 A PERSPECTIVE ON NEW GENERATION OF SUPER-SCALAR RISC PROCESSORS, Honeywell-Bull Group User Seminar, Budva, Yugoslavia, September 21, 1995.

82. 1995 NEW DIFFERENTIAL LOGIC BASED ON PASS-TRANSISTOR DESIGN, Ecole Superieure d'Ingenieurs en Electrotechnique et Electronique, Noisy le Grand, FRANCE, September 26, 1995.

83. 1996 ADVANCED LOGIC DESIGN: METHODOLOGY AND CIRCUIT TECHNIQUES, Series of lectures, Hewlett-Packard Laboratories, Palo Alto, February-April, 1996

84. 1996 ADVANCED LOGIC DESIGN: METHODOLOGY AND CIRCUIT TECHNIQUES, series of lectures, Fudan University, Shanghai, P.R. CHINA, April 22-26, 1996.

85. 1996 LA HISTORIA DEL DESARROYO DE SYSTEMAS DE COMPUTACION Y LA PROYECTION POR EL FUTURO, Universidad San Francisco Xavier de Chuquisaca , Sucre, BOLIVIA, Septiembre 24, 1996.

86. 1997 MODERN MICROPROCESSOR ARCHITECTURES, Intel Corporation, Beaverton, Oregon, January 27, 1997.

87. 1997 MODERN MICROPROCESSOR ARCHITECTURES, Digital Equipment Corporation, Hudson, Massachusetts, January 31, 1997.

88. 1997 MODERN MICROPROCESSOR ARCHITECTURES: Evolution of RISC into Super-Scalars, Tutorial given at the International Solid-State Circuits Conference, San Francisco, California, February 5, 1997.

89. 1997 ALGORITHM FOR EFFICIENT IMPLEMENTATION OF FAST PARALLEL MULTIPLIERS, Seminar given at Silicon Graphics Incorporated, Mountain View, California, February 19, 1997.

90. 1997 DEVELPMENT OF FAST VLSI DATA-PAHTS, Compass Design Automation, San Jose, California, March 5, 1997.

91. 1997 ALGORITHMS FOR GENERATION OF HIGH-SPEED DATA-PATH COMPILERS, Cascade Design Automation, Bellevue, Washington, March 13, 1997.

92. 1997 MAPPING OF ALGORITHMS INTO TECHNOLOGY: HIGH-SPEED DATA-PATH IMPLEMENTATION, LSI Logic Corporation, Milpitas, California, April 7, 1997.

93. 1997 LOW-POWER DESIGN TECHNIQUES IN VLSI SYSTEMS, Seminar at Hewlett-Packard Company Internal Workshop, Monterey, California, May 27, 1997.

94. 1997 ADIABATIC TECHNIQUES FOR ACHIEVING LOW-POWER: EXPERIMENTAL RESULTS, Tokyo University, Tokyo, JAPAN, June 10, 1997.

95. 1997 CLOCKING METHODOLOGY AND LATCH DESIGN TECHNIQUES FOR LOWPOWER PROCESSORS, Hitachi Central Research Laboratories, Kokubunji, Tokyo, JAPAN, June 16, 1997.

96. 1997 MODERN MICROPROCESSOR ARCHITECTURES: DEVELOPMENT THAT LED TO SUPER-SCALAR IMPLEMENTATIONS, SONY Corporate Headquarters, Tokyo, JAPAN, June 17, 1997.

97. 1997 IMPACT OF MULTI-MEDIA COMPUTING ON COMPUTER ARITHMETIC: IS THERE A NEED FOR STANDARDISATION? Panel Presentation, 13th International Symposium on Computer Arithmetic, Asilomar, California, July 8, 1997.

98. 1997 DIFFERENTIAL AND PASS-TRANSISTOR CMOS LOGIC FOR HIGHPERFORMANCE SYSTEMS, *21st International IEEE Conference on Microelectronics*, September 15-17, 1997, Nis, Yugoslavia.

99. 1997 AN APPLICATION OF DYNAMIC PROGRAMMING TO THE DESIGN OF A FAST ARITHMETIC LOGIC UNIT, AT&T Seminar Series, Department of Industrial Engineering, Georgia Institute of Technology, Atlanta, Georgia, October 6, 1997.

100. 1998 COMPARATIVE STUDY OF THE ADVANCED LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOW-POWER VLSI SYSTEMS, Sun Microsystems Laboratories, Sunnyvale, California, February 26, 1998.

101. 1998 ADVANCED LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOWPOWER VLSI SYSTEMS, Internal Symposium on Low Power Design, Micro-Computer Research Laboratories, Intel Corporation, Hillsboro, Oregon, February 10, 1998.

102. 1998 VLSI ARITHMETIC FOR LOW-POWER VLSI SYSTEMS, Internal Symposium on Low Power Design, Micro-Computer Research Laboratories, Intel Corporation, Hillsboro, Oregon, February 10, 1998.

103. 1998 SUPER-SCALAR PROCESSOR ARCHITECTURE, Center for Integrated Systems, Korea Advanced Institute of Science and Technology - KAIST, Taejon, KOREA, May 22, 1998.

104. 1998 SUPER-SCALAR PROCESSOR ARCHITECTURE, Seoul National University, Seoul, KOREA May 25, 1998.

105. 1998 ARCHITECTURAL TRADEOFFS FOR LOW POWER, The 25th Annual International Symposium on Computer Architecture - ISCA, Barcelona, SPAIN June 28, 1998.

106. 1999 ADVANCED LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOWPOWER VLSI SYSTEMS, Computer Elements Workshop, Mesa Arizona, January 18, 1999.

107. 1999 ARITHMETIC UNITS FOR DSP AND MEDIA SIGNAL PROCESSING, MEAD DSP course, Monterey, March 9, 1999.

108. 2000 COMPARATIVE ANALYSIS OF MASTER-SLAVE LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, IBM Austin Research Center, Austin, Texas, February 18, 2000.

109. 2000 ADVANCED LOGIC DESIGN, Berkeley Summer Institute, University of California, Berkeley, June 7-9, 2000.

110. 2000 DESIGN TECHNIQUES FOR LOW POWER, ST Microelectronics, Grenoble, FRANCE, July 31, 2000.

111. 2000 CLOCKED TIMING ELEMENTS IN HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, ST Microelectronics, La Jolla, California, November 6, 2000.

112. 2001 VLSI ARITHMETIC, Online Symposium for Electronics Engineers (OSEE), scheduled to be aired, 5pm EST (22pm GMT), January 23, 2001.

113. 2001 PROCESSOR DESIGN CHALLENGES, Microprocessor Design Workshop, International Solid-State Circuits Conference, San Francisco, February 8, 2001.

114. 2001 CLOCKED TIMING ELEMENTS FOR HIGH-PERFORMANCE AND LOW POWER VLSI SYSTEMS, IBM Sponsored Computer Architecture Seminar Series, University of Texas at Austin, February 12, 2001.

115. 2001 COMPUTATIONAL REQUIREMENTS FOR MEDIA SIGNAL PROCESSING, Electrical and Computer Engineering Department, University of Texas at Austin, February 12, 2001.

116. 2001 CLOCKED STORAGE ELEMENTS: MASTER-SLAVE LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, Ecole Superieure d'Ingenieurs en Electrotechnique et Electronique - ESIEE, Paris, FRANCE, March 21, 2001.

117. 2001 CLOCKED STORAGE ELEMENTS: MASTER-SLAVE LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, Barcelona, SPAIN, March 23, 2001.

118. 2001 VLSI ARITHMETIC ADDERS AND MULTIPLIERS, 29ème École de Printemps d'Informatique Théorique: Arithmétique des Ordinateurs, Prapoutel-Les-Sept-Laux, FRANCE, March 26, 2001.

119. 2001 CLOCKED STORAGE ELEMENTS: MASTER-SLAVE LATCHES AND FLIP-FLOPS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, TIMA, Grenoble, FRANCE, March 28, 2001.

120. 2001 HIGH-SPEED VLSI ARITHMETIC UNITS: ADDERS AND MULTIPLIERS, Electrical Engineering Department Colloquia, University of California Los Angeles, May 10, 2001.

121. 2001 TIMING ELEMENTS AND TIMING ISSUES IN HIGH-PERFORMANCE PROCESSORS, Event sponsored by CAS Distinguished Lecturer Program and by IEEE French Section, Institut Supérieur d'Electronique de Paris, Paris, FRANCE, May 29, 2001.

122. 2001 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Event sponsored by CAS Distinguished Lecturer Program and by IEEE French Section, Institut Supérieur d'Electronique de Paris, Paris, FRANCE, May 29, 2001.

123. 2001 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, IEEE Workshop on Low-Power Design, FTFC 2001: Faible Tension Faible Consommation, Paris, FRANCE, May 30 – June 1st, 2001.

124. 2001 WILL START-UPS OUTPERFORM BIG COMPANIES? Panel Presentation, IEEE, 2001 Symposium on VLSI Circuits, Righa Royal Hotel Kyoto, Kyoto, JAPAN, June 14, 2001.

125. 2001 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE APPLICATIONS, Fujitsu Laboratories, Kawasaki, Tokyo, JAPAN, June 18, 2001.

126. 2001 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOWPOWER SYSTEMS, Invited Tutorial given at the International Conference on Computer Design, ICCD 2001, Austin, Texas, September 24, 2001.

127. 2002 DESIGN OF CLOCKED STORAGE ELEMENTS, Center for Integrated Systems, Stanford University, California, January 22, 2002.

128. 2002 DESIGN OF CLOCKED STORAGE ELEMENTS, Dean's Seminar, College of Engineering, University of California, Santa Cruz, California, January 31, 2002.

129. 2002 DESIGN OF SEQUENTIAL ELEMENTS, ISSCC Microprocessor Design Workshop: "High-Frequency Clocking - Issues and Solutions for Clocking High-Frequency Microprocessors," Thursday, February 7th, 2002, San Francisco.

130. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Invited Lecture, University of Hawaii at Manoa, Honolulu, Hawaii, March 20, 2002.

131. 2002 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, IEEE CAS Distinguished Lecture, IEEE Section, Honolulu, Hawaii, March 21, 2002.

132. 2002 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOW-POWER SYSTEMS, Invited Tutorial given at the IEEE Solid-State Circuits Chapter Meeting, Dallas, Texas, March 25, 2001.

133. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER-SCALARS, Invited Lecture, Electrical Engineering Colloquium, Department of Electrical Engineering, University of Texas at Dallas, March 26, 2002.

134. 2002 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, Invited Lecture, Electrical and Computer Engineering Department, University of Texas at Austin, Austin, Texas, March 27, 2002.

135. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Invited Lecture, Department of Electronics Computer Science and Systems, University of Calabria, Arcavacata di Rende, RENDE, ITALY, April 23, 2002.

136. 2002 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, Invited Lecture, Department of Electronics Computer Science and Systems, University of Calabria, Arcavacata di Rende, RENDE, ITALY, April 24, 2002.

137. 2002 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, Invited Lecture, ST Microelectronics, Research and Development Division, Catania, ITALY, April 30, 2002.

138. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Distinguished Lecture, Electrical Engineering and Computer Sciences Department, University of Novi Sad, Novi Sad, YUGOSLAVIA, May 9, 2002.

139. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Distinguished Lecture, Electrical Engineering Department, University of Belgrade, Belgrade, YUGOSLAVIA, May 10, 2002.

140. 2002 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, Distinguished Lecture, Electrical Engineering Department, University of Belgrade, Belgrade, YUGOSLAVIA, May 10, 2002.

141. 2002 HIGH-SPEED VLSI ARITHMETIC UNITS: ADDERS AND MULTIPLIERS, Distinguished IEEE Solid-State Circuits Society Lecture, Electrical Engineering Department, University of Nis, Nis, YUGOSLAVIA, May 13, 2001.

142. 2002 MODERN MICROPROCESSOR ARCHITECTURES: EVOLUTION OF RISC INTO SUPER SCALAR, Distinguished IEEE Solid-State Circuits Society Lecture, Electrical Engineering Department, University of Nis, Nis, YUGOSLAVIA, May 13, 2001.

143. 2002 A METHOD FOR SPEED OPTIMIZED PARTIAL PRODUCT REDUCTION AND GENERATION OF FAST PARALLEL MULTIPLIERS USING AN ALGORITHMIC APPROACH, Intel Microprocessor Research Laboratories, Hillsboro, Oregon, August 1, 2002.

144. 2002 FUTURE DIRECTIONS IN CLOCKING MULTI-GHZ SYSTEMS, Invited Talk, International Symposium on Low-Power Electronics and Design, Monterey, California, August 12-14, 2002.

145. 2002 CLOCKED STORAGE ELEMENTS IN MULTI-GHZ DESIGN, Intel Microprocessor Research Laboratories, Hillsboro, Oregon, August 23, 2002.

146. 2002 ENERGY-DELAY ESTIMATION TOOL AND ANALYSIS: APPLICATION ON REPRESENTATIVE VLSI ADDER TOPOLOGIES, Intel Microprocessor Research Laboratories, Hillsboro, Oregon, August 23, 2002.

147. 2002 PERFORMANCE COMPARISON OF VLSI ADDERS USING LOGICAL EFFORT, Invited Talk, 12th International Workshop on Power and Timing Modeling, Optimization and Simulation - PATMOS 2002, Seville, Spain, September 11 - 13, 2002.

148. 2002 CLOCKING AND CLOCKED STORAGE ELEMENTS IN GHZ ENVIORMNENT, Instituto de Microelectrónica de Sevilla, E.T.S.I. Informática, Centro Nacional de Microelectrónica, Universidad de Sevilla, Sevilla, SPAIN, September 16, 2002.

149. 2002 MODERN MICROPROCESSOR ARCHITECTURES, IEEE Distinguish Lecture, University of Patras, Patras, GREECE, December 16, 2002.

150. 2002 MODERN MICROPROCESSOR DEVELOPMENT PERSPECTIVE, Keynote Address, 25th Anniversary of the Electrical Engineering Department, University of Banja Luka, Banja Luka, Serbian Republic, December 21, 2002.

151. 2003 OPTIMIZING HIGH-PERFORMANCE DIGITAL CIRCUITS IN ENERGY CONSTRAINED ENVIRONMENT, Invited Presentation, 4eme journes d'etudes Faible Tension Faible Consummation, FTFC'2003, Cercle National des Armees, Paris, FRANCE, May 15, 2003.

152. 2003 DESIGN OF POWER EFFICIENT VLSI ARITHMETIC: SPEED AND POWER TRADE-OFFS, Invited Tutorlal, 16th IEEE Symposium on Computer Arithmetic, Santiago de Compostela, SPAIN, June 15-18, 2003.

153. 2003 OPTIMZING HIGH-PERFORMANCE DIGITAL CIRCUITS IN ENERGY CONSTRAINED ENVIRONMENT, Instituto de Informatica, Grupo de Arquitectura de Computadores, Escuela Tecnica Superior Ingenieria, Universidad de Santiago de Compostela, Santiago de Compostela, SPAIN, June 20, 2003.

154. 2003 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOWPOWER SYSTEMS, IEEE Distinguished Lecture, Microelectronic Systems Laboratory, Institute of Microelectronics and Microsystems, Switzerland (West) Chapter of IEEE Solid-State Circuits Society, Swiss Federal Institute of Technology, Lausanne, SWITZERLAND, June 23, 2003.

155. 2003 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOWPOWER SYSTEMS, Samsung LSI Research Laboratories, Seoul, KOREA, September 5, 2003.

156. 2003 MICROPROCESSOR DEVELOPMENT PERSPECTIVE, IEEE Distinguished Lectures Series, Korea IEEE Solid-State Circuits Chapter, Korea University, Seoul, KOREA, September 17, 2003.

157. 2003 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOWPOWER SYSTEMS, Center for Embedded Systems, Seoul National University, Seoul, KOREA, October 7, 2003.

158. 2003 MICROPROCESSOR DEVELOPMENT PERSPECTIVE, IEEE Distinguished Lecture, China IEEE Solid-State Circuits Chapter, Beijing Branch, Institute of Microelectronics, Tsinghua University, Beijing, P.R. CHINA, October 20, 2003.

159. 2003 FUTURE DIRECTIONS IN CLOCKING MULTI-GHZ SYSTEMS, Microprocessor R&D Center, Department of Computer Science, Peking University, Beijing, P.R. CHINA, October 22, 2003.

160. 2003 BALANCING BETWEEN DESIGN AND DESIGN AUTOMATION, Invited, Panel Discussion Presentation, 5th International Conference on ASIC, Beijing, P.R. China, October 23, 2003.

161. 2003 MULTI GHZ SYSTEM CLOCKING, Invited Presentation, 5th International Conference on ASIC, Beijing, P.R. China, October 24, 2003.

162. 2003 POWER EFFICIENT VLSI ARITHMETIC: SPEED AND POWER TRADE-OFFS, IEEE Seoul Solid-State Circuits Chapter Distinguished Lecture, School of Electrical and Electronic Engineering, Yonsei University, Seoul, KOREA, October 31, 2003.

163. 2003 ENERGY MINIMIZATION METHOD FOR OPTIMAL ENERGY-DELAY, Fujitsu Research Laboratories, Kawasaki, JAPAN, December 3, 2003.

164. 2003 CLOCKED STORAGE ELEMENTS IN HIGH-PERFORMANCE AND LOW-POWER PROCESSORS, Hitachi Research Laboratories, Kokubunji, JAPAN, December 5, 2003.

165. 2003 MICROPROCESSOR DEVELOPMENT PERSPECTIVE, IEEE Distinguished Lecture, Fudan University, Shanghai, P.R. CHINA, December 25, 2003.

166. 2003 MICROPROCESSOR DEVELOPMENT PERSPECTIVE, Institute of VLSI Design, Zhejiang University, Hangzhou, P.R. CHINA, December 26, 2003.

167. 2003 POWER EFFICIENT VLSI ARITHMETIC, Departamento de Tecnología Electrónica, Universidad de Sevilla, Sevilla, SPAIN, May 6, 2003.

168. 2004 CLOCKING MULTI-GHZ SYSTEMS, Departamento de Tecnología Electrónica, Universidad de Sevilla, Sevilla, SPAIN, May 7, 2004.

169. 2004 ENERGY-DELAY RELATIONSHIP IN DIGITAL CIRCUITS DESIGN, Invited presentation, 24th IEEE International Conference on Microelectronics, Nis, SERBIA, May 18, 2004

170. 2004 POWER EFFICIENT DESIGN: SPEED AND POWER TRADE OFFS, Laboratoire del'Informatique du Parallélisme, Ecole Normale Superieure de Lyon, Lyon, FRANCE, June 17, 2004.

171. 2004 ENERGY MINIMIZATION METHOD FOR OPTIMAL ENERGY-DELAY, "Leakage, Energy and Speed in Digital Circuits" advanced seminar organized by TIMA Laboratory, Grenoble, France, June 15, 2004.

172. 2004 ENERGY MINIMIZATION FOR OPTIMAL ENERGY-DELAY, Infineon, Munich, GERMANY, June 23, 2004.

173. 2004 CLOCKED STORAGE ELEMENTS FOR HIGH-PERFORMANCE AND LOWPOWER SYSTEMS, Infineon, Munich, GERMANY, June 23, 2004.

174. 2004 DIGITAL CIRCUITS OPTIMIZATION IN ENERGY-DELAY SPACE, Intel Advanced Microprocessor Research Laboratory, Hillsboro, Oregon, December 6, 2004.

175. 2005 CLOCKING OF DIGITAL SYSTEMS FOR HIGH-PERFORMANCE AND LOWPOWER, Tutorial Presentation, International Symposium on Circuits and Systems, Kobe, JAPAN, May 23, 2005.

176. 2005 DESIGNING ENERGY EFFICIENT CMOS CIRCUITS, SRC Forum, June 24, 2005.

177. 2005 ENERGY-DELAY TRADE-OFF IN CMOS DIGITAL CIRCUITS DESIGN, National Chiao Tung University, Hsinchu, Taiwan, June 30, 2005.

178. 2005 DESIGNING ENERGY EFFICIENT CMOS CIRCUITS, School of Electrical and Computer Engineering, Royal Melbourne Institute of Technology, Melbourne, Victoria, AUSTRALIA, July 8, 2005.

179. 2005 DESIGNING ENERGY EFFICIENT CMOS CIRCUITS, Department of Electrical and Electronic Engineering seminar, The University of Melbourne, Victoria, AUSTRALIA, July 8, 2005.

180. 2005 ENERGY-DELAY TRADE-OFF IN CMOS DIGITAL CIRCUITS, School of Electrical and Electronic Engineering, The University of Adelaide, Adelaide, AUSTRALIA, July 26, 2005.

181. 2005 DESIGNING ENERGY EFFICIENT CMOS CIRCUITS, Presentation at the meeting of the Swedish Foundation for Strategic Research, Linkoping, SWEDEN, August 25, 2005.

182. 2005 LOW POWER DESIGN OF CMOS DIGITAL CIRCUITS, IEEE Solid-State Distinguished Lecture, IEEE-SSC Sweden Chapter, Linkoping University, SWEDEN, August 26, 2005.

183. 2005 DIGITAL SYSTEM CLOCKING: High-Performance and Low-Power Aspects, Invited Tutorial, 8th EUROMICRO Conference on Digital System Design, Porto, PORTUGAL, August 30, 2005.

184. 2005 LOW-POWER DESIGN METHODOLOGY FOR CMOS DIGITAL CIRCUITS: APPLICATION TO STANDARD LIBRARIES: Presentation at UMC, Hsinchu, TAIWAN, September 30, 2005.

185. 2005 ENERGY-DELAY TRADE-OFF IN CMOS DIGITAL CIRCUITS DESIGN, Presentation at Dallas IEEE CAS Workshop, Richardson, Texas, October 10, 2005.

186. 2005 CLOCK SKEW ABSORBING FLIP-FLOP DESIGN AND DIGITAL TIMING PARTITION, Tutorial Presentation, UMC, Hsinchu, TAIWAN, October 31, 2005.

187. 2005 ENERGY-EFFICIENT OPTIMIZATION OF THE VITERBI ACS UNIT ARCHITECTURE, Presentation at the 1st Asian Solid-State Circuits Conference, Hsinchu, TAIWAN, November 2, 2005.

188. 2006 MICROPROCESSOR DEVELOPMENT: RETROSPECTIVE AND FUTURE CHALLENGES, Invited presentation, School of Information Technology, Sydney University, Sydney, AUSTRALIA, July 12, 2006.

189. 2006 FUTURE OF MICROPROCESSORS: RETROSPECTIVE AND CHALLENGES, IEEE Distinguished Lecture, IEEE Western Australia Section. ICT Innovation Centre, Perth, AUSTRALIA, November 6, 2006.

190. 2006 DIRECTIONS IN COMPUTER ENGINEERING, Keynote Presentation, The Seventh Postgraduate Electrical Engineering and Computing Symposium, PEECS 2006, Murdoch University, Perth, Western Australia, November 7, 2006.

191. 2006 VLSI ARITHMETIC: METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, IEEE Distinguished Lecture, Fudan University, Shanghai, P.R. China, November 16, 2006.

192. 2006 VLSI ARITHMETIC: METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***IEEE Distinguished Lecture,*** Tsinghua University, Beijing, P.R. China, November 18, 2006.

193. 2007 ENERGY-DELAY TRADE-OFFS IN CMOS DIGITAL CIRCUITS DESIGN: Cadence Berkeley Research Laboratory, Berkeley, February 9, 2007.

194. 2007 MICROPROCESSOR DEVELOPMENT: RETROSPECTIVE AND FUTURE CHALLENGES, Invited presentation, Department of Computer Science, University of Otago, Dunedin, New Zealand, April 17, 2007.

195. 2007 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, IEEE and HKN Distinguished Lecture, Department of Electrical Engineering, University of Texas at San Antonio, San Antonio, Texas, November 16, 2007.

196. 2008 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, Department of Electrical Engineering, University of Belgrade, Belgrade, SERBIA, May 16, 2008.

197. 2008 DIRECTIONS IN COMPUTER ENGINEERING, Department of Electrical Engineering, University of Belgrade, Belgrade, SERBIA, May 20, 2008.

198. 2008 LOW-POWER DESIGN AND ENERGY-DELAY RELATIONSHIP IN DIGITAL SYSTEMS, ***IEEE Distinguished Lecture,*** Department of Electrical Engineering, Bogazici University, Istanbul, TURKEY, May 29, 2008.

199. 2008 LOW-POWER DESIGN AND ENERGY-DELAY RELATIONSHIP IN DIGITAL SYSTEMS, ***IEEE Distinguished Lecture,*** Department of Electrical Engineering, Istanbul Technical University, Istanbul, TURKEY, May 29, 2008.

200. 2008 MICROPROCESSOR DEVELOPMENT: RETROSPECTIVE AND FUTURE CHALLENGES, ***Keynote Speaker,*** IEEE International Conference on Microelectronics, ICM 2008, Sharjah University, Sharjah, United Arab Emirates, December 15, 2008.

201. 2008 LOW-POWER DESIGN TECHNIQUES, ***Invited Speaker,*** Engineering Department, University of Sharjah, United Arab Emirates, December 16, 2008.

202. 2009 LOW-POWER DESIGN OF CMOS DIGITAL CIRCUITS, Taiwan Semiconductor Manufacturing Corp. - TSMC, Hsinchu, TAIWAN, May 26, 2006.

203. 2009 LOW-POWER DESIGN TECHNIQUES IN DIGITAL SYSTEMS, ***Invited Tutorial,*** IEEE Midwest Symposium on Circits and Systems, Cancun, MEXICO, August 2, 2009.

204. 2009 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***Invited Lecture,*** Computer Engineering Colloquium, TU Delft - Delft University of Technology, Delft, THE NETHERLANDS, September 9, 2009.

205. 2009 A NEW METHODOLOGY FOR POWER-AWARE TRANSISTOR SIZING: FREE POWER RECOVERY (FPR), PATMOS 2009, Delft, THE NETHERLANDS, September 11, 2009.

206. 2009 COMPUTING AT THE ULTIMATE LOW-ENERGY LIMITS, ***Invited Lecture,*** CMOS Emerging Technologies Workshop, CANADA, September 25, 2009.

207. 2009 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***IEEE Distinguished Lecture,*** IEEE Solid-State Circuits Society, Germany Chapter, Hanover University, Hanover, GERMANY, October 7, 2009.

208. 2009 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***IEEE Distinguished Lecture,*** IEEE Solid-State Circuits Society, Ireland Chapter, Tyndall National Institute and the University of Cork, IRELAND, October 9, 2009.

209. 2009 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***Invited Speaker,*** The Hong-Kong University of Science and Technology, Hong-Kong, October 19, 2009.

210. 2010 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***IEEE Distinguished Lecture,*** IEEE Solid-State Circuits Society, Santa Clara Valley Chapter, April 15, 2010.

211. 2010 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, Southern Methodist University, Computer Science and Engineering Seminar, Dallas, Texas, April 22, 2010.

212. 2010 LOW-POWER DESIGN, Euro Program Short Course, Engineering Department, University of Bologna, Bologna, ITALY, May, 24-27, 2010.

213. 2010 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, Advanced Micro Devices, Austin, Texas, August 20, 2010.

214. 2010 ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***Invited Tutorial,*** *23rd Symposium on Integrated Circuits and System Design*, Bourbon Convention Center, Ibirapuera, Sao Paolo, BRAZIL, September 6, 2010.

215. 2010 COMPUTING AT THE ULTIMATE LOW-ENERGY LIMITS, ***Invited paper,*** *23rd Symposium on Integrated Circuits and System Design*, Bourbon Convention Center, Ibirapuera, Sao Paolo, BRAZIL, September 6, 2010.

216. 2011 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***IEEE Distinguished Lecture,*** IEEE Solid-State Circuits & IEEE CAS Chapter, Porto Alegre, BRAZIL, May 20, 2011.

217. 2011 A QUICK METHOD FOR ENERGY OPTIMIZED GATE SIZING OF DIGITAL CIRCUITS, *21st International Workshop, PATMOS 2011 on Power and Timing Modeling, Optimization, and Simulation*, Madrid, SPAIN, September 27, 2011.

218. 2011 MICROPROCESSOR DEVELOPMENT: RETROSPECTIVE AND FUTURE CHALLENGES, *Seminar*, Universidad Pontificia Comilla's, Madrid, SPAIN, September 30, 2011.

219. 2012 METHODOLOGY FOR ENERGY-EFFICIENT DESIGN OF DIGITAL CIRCUITS, ***Invited Presentation***, Conferencia Argentina de Micro-Nanoelectrónica, Tecnologías y sus Aplicaciones – CAMTA, Córdoba, Argentina, Augusto 9, 2012

220. 2012 LOW-POWER DESIGN IN 5 EASY STEPS, Short Course given at: Conferencia Argentina de Micro-Nanoelectrónica, Tecnologías y sus Aplicaciones – CAMTA, Córdoba, Argentina, Augusto 9, 2012.

221. 2012 IEEE CIRCUITS AND SYSTEMS: NEW PERSPECTIVES AND VISION, Simposio Argentino de Sistemas Embebidos, SASE 2012, Facultad de Ingeniería - Universidad de Buenos Aires, Buenos Aires, Argentina, Augusto 15, 2012.

222. 2015 MINIMIZING ENERGY BY ACHIEVING OPTIMAL SPARSENESS IN PARALLEL ADDERS, 22nd IEEE Symposium on Computer Arithmetic, Lyon, FRANCE, June 22-24, 2015.