# Steve Novak

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**Professional Summary:** Strong technical and business leader for entire Digital Design and chip integration flow. Proven track record of managing dispersed and efficient teams and delivering successful silicon and system success in large and small company environments. .He has developed and performed the design and verification of ASIC/SOC/FPGA systems including memory controllers(SDRAM, DDR), high speed communication interfaces (PCIe, SATA, USB), wireless devices, and a wide range of peripherals. He holds a bachelor's degree in Electrical Engineering and Master's degree in Computer Science from University of California, Los Angeles.


**Areas of experience**: Ethernet(10/40/100, 10Gb Xaui, XFI), Memory controllers(SRAM, DRAM, DDR) protocols and designs. Basic Cryptography, FEC (Forward Error Correction), MAC(Media Access Controller) for DOCSIS and 802.11. Intel, ARM (AHB bus – AXI, AHB, APB), Power PC, MIPS microprocessor architectures, GPU architectures and chipsets, MCU integration, most common protocols (PCI, USB, Ethernet, I2C, SATA, SPI, DP AUX, JTAG), LIDAR sensor, MIPI , AI systems and processors

## Experience

### 2008 – present Bay2Sierra Silicon Services

***Principal engineer, Consulting and Contracting Services***

- IP services
  - IP portfolio review and evaluation
  - Reads patents to understand infringement and validity issues
  - Examines software source code for determining patent infringement
  - Examines HDL code (e.g., Verilog and VHDL) for determining patent infringement
  - Examines schematics for determining patent infringement
  - Write expert reports
- ASIC/FPGA architecture, design, verification and physical implementation
  - PCS/MAC layer for Ethernet, PCIe, SATA,
  - Memory(DDR3)/Flash (NAND and NOR), MRAM controller design and verification
  - FEC (Forward Error Correction)
  - Smart Meter ASIC architecture and design including wireless communication solution
  - NFC (Near Field Communication) – 60GHZ wireless high bandwidth USB solution.
  - Security/cryptography IP development and integration
  - 10/40/100G (MLG, GBOX) ethernet repeater
  - AHB2AXI and AXI2AHB bridges for on-chip networks
  - Communication protocols - USB, PCIe, SATA, PCI, I2C, DP AUX, SPI, MIPI, JTAG.
  - SOC (System On Chip) architecture and development (smart meter, RFID, switch/networking/compute centric chips)
- Project flow and methodology review
- Business and acquisition plan review
- Evaluation of IP and RTL code re-usability
- Verification of the integration of cryptography IP
- Some of our Past Clients: AMD, Avicena, Impinj, Indie Semi, Keyssa, Meta Inc, NetApp, Netspeed, PMC Sierra, Silicon Image, SilverSpring Networks, Spansion, Xilinx

### 2006 – 2008 Keyeye Communications

- Director Digital Design
- ASIC design for 10G 802.3an phy (10G Ethernet over twisted pair copper) design which was optimized for low power and had multiple power domains.
- Managed (6 direct reports) and technically lead digital architecture, design, and backend implementation.

- Responsible for fullchip design flow, methodology and automation; chip schedule and integration. Integrated multiple internally generated Analog blocks into fullchip digital design/simulation and P&R flow.

## 2002 – 2006 Fulcrum Microsystems

***Chip Lead*** *Calabasas, Ca*

- Chip lead for FocalPoint, a low latency layer 2 24 port 1/10Gb Ethernet switch (200ns latency, 240Gb throughput.). Worked on second generation layer 3 switch. FocalPoint in successful production. FPGA and board prototyping and reference design. Responsible for digital logic architecture and implementation; IP relationships and selection; and backend vendor selection and management
- Lead architecture and implementation for all Synchronous blocks on **SPI4 switch chip**. Involved in all aspects of the chip's development – architecture, design, verification, P+R, test.

## 2000 – 2002 Juniper Networks/Pacific Broadband Communications

- Senior ASIC designer
- Performance and verification work on DOCSIS 1.1 CMTS ASIC.

*7/2000 – 102001: Paris, France*

- Architected MAC for **DOCSIS 1.1 CMTS** (Cable Modem Termination ).
- Led group of 4 people to implement, verify in simulation and in a FPGA the entire MAC and parts of the DSP.
- Work included creation of the verification environment, coordination with Software of the HW/SW split, timing closure, and ultimately testing the finished product.

## 1993 - 2000 Advanced Micro Devices

***Member Technical Staff***

*1999- 2000 Dresden, Germany*

- Co-Led Architecture and initial implementation for an **802.11b MAC** and BBP(BaseBand Processor) with team of 5 designers.
- Developed the architecture and RTL for a DMA controller for an ADSL chipset.

*1998-1999 Austin, Texas*

- Worked on the PCI interface for **AMD Ethernet product** and also finished the architecture, implementation and physical design of the DDR memory controller for the AMD k7 chipset.

*1997-1998 Sunnyvale, California*

- Team lead for **K7 chipset**. Specifically in charge of the SDRAM memory controller.
- NorthBridge architecture, chip and system design, back-end physical design, verification flow and ASIC lab debug.

*1995-1997 Milpitas, California*

- FPU adder and multiplier (Wallace Tree) pipeline for a new X86 FPU(hand instantiated gate and placement).
- Responsible for architecting and implementing IO, clock block support, part of the scheduler and various pieces of logic and microcode throughout the design(design, verification, debug, timing, routing and placement) for **K6 microprocessor**.

*1993- 1995 Austin, Texas*

- Development of the **Am486 SLE** series Intel compatible write back cache processors – development SLE microcode..

## Legal Consulting

I have consulted on a total of 12 litigations. I have provided expert testimony once at deposition and provided a expert tutorial in court.

1/2023-current: ongoing Network on a chip and block chain cases

**10/2021 – 04/2023 Viasat Inc., Ltd v. Kioxia Corp and Western Digital Corp**

Law Firm: Bartlit Beck LLP
Client: Viasat
Case: 6:21-cv-01231-ADA and 6:21-cv-01230-ADA

- Nand Flash ECC encoder/decoder patents – claim charts and code review

**11/2022 – 01/2023 Samsung Elecontronics Co., Ltd v. Netlist, Inc**

Law Firm: Irell & Manella LLP
Client: Netlist
Case: IPR IPR2022-00615 – external memory (DDR DRAM) optimization patents

- Helped develop POPR – Patent Owner's Preliminary Response

**02/2021 – 06/2022 Zentian LTD, v. Apple Inc. and Amazon.com, Inc.**

Law Firm: Bartlit Beck LLP
Client: Zentian
Case: C.A. No. 6:22-cv-122 and C.A. No. 6:22-cv-00123

- Smart speakers and Speech Recognition patent review and claim charts

**1/2020-3/2021: American Arbitration Association Adeniyi Abiodun case v. Peernova Inc.; Open-Silicon, Inc**

Law Firm: John Claassen, Esq
Client: PeerNova; Open-silicon, Inc
Case: 01-18-0002-9329

- Bitcoin project – deposed for this case

**05/2020 - 08/2020 - TEXAS INSTRUMENTS INC. V. VANTAGE MICRO, LLC**

Law Firm: Devlin Law Firm LLC
Client: Vantage Micro. LLC
**Case: IPR2020-00830**
**U.S. Patent No. 7,414,606 – "**Method and apparatus for detecting a flat panel display monitor" Plug and play with display connection using VESA and USB standards.

- Wrote POPR declaration report

**8/2019- 10/2019: EXEGY INCOPORATED and IP RESERVOIR LLC v. ACTIV FINANCIAL, INC**

Law Firm: Harness, Dickey & Pierce P.L.C and Nixon Peabody, LLP.
Client: Exegy Inc
Court: Northern District of Illinois
Case: 1:19-cv-02858

- Code(Verilog and C++) review of FPGA acceleration of financial market data
- Develop expert report

**7/2018 – 11/2018: USB Bridge Solutions v. Buffalo and Avant Technology**

Law Firm: Kheyfits Belenky LLP
Client: USB Bridge solutions
Court: Western District of Texas Austin division
Case: 1:17-cv-001158-LY

- Alleged patent infringement of ATA to USB bridge technology
- Testifying expert
- Gave technical brief in court

**11/2018 – 3/2019: Complex Memory v. ZTE Corporation and ARM**

Law Firm: Toler Law Group
Client: complex memory LLC
Court: IPR
Case: IPR2019-0053/0058

- Alleged patent infringement of buffered DRAM technology
- Wrote an expert declaration

**1/2016 – 3/2016: Oracle vs. Google**

Law Firm: Orrick, Herrington & Sutcliffe
Client: Oracle America
Court: U.S. District Court, Northern District of California
Case: C 10-03561 WHA

- Alleged copyright of software APIs

- Analyzed API use cases

**1/2015 – 8/2015: NVidia Corporation vs. Samsung Electronics, Qualcomm Inc.**
Law Firm: Orrick, Herrington & Sutcliffe LLP
Client: NVidia Corporation
Court: U.S. International Trade Commission
Case: Inv. No. 337-TA-932

- Testifying expert
- Alleged patent infringement of GPU integrated circuits
- Examined HDL code
- Expert report pertaining to source code analysis

## Education

***Masters Business Administration,*** *2009 Golden Gate University San Francisco, California*

***Masters in Computer Science***, *1993 University of California Los Angeles, California*

***Bachelor of Science in Electrical Engineering***, 1991 University of California Los Angeles, California

## Patents:

Named inventor on 13 patents:

1. Michel A. Moacanin, Jeremy Boulton, Steven Novak, "Methods and apparatus for providing test access to asynchronous circuits and systems," U.S. Patent 7,260,753
2. Stephan Rosner, William F. Kern, Ralf Flemming, Matthias Baer, Stephen T. Novak, "Wireless computer system with queue and scheduler" U.S. Patent 7,149,213
3. Benoit Marleux, Steven Novak, "Context switching for on-the-fly processing of fragmented frames." U.S. Patent 7,089,486
4. Stephan Rosner, Jörg Winkler, Ralf Flemming, Stephen T. Novak, "Method and apparatus for accessing memories having a time-variant response over a PCI bus by using two-stage DMA transfers" U.S. Patent 7,047,328
5. Stephen T. Novak, Scott Waldron, John C. Peck, Jr., "Queue based memory controller" U.S. Patent 6,496,906
6. Stephen T. Novak, John C. Peck, Jr., "Queue based data control mechanism for queue based memory controller" U.S. Patent 6,393,531
7. Stephen T. Novak, John C. Peck, Jr., "Method and apparatus for optimizing memory performance with opportunistic pre-charging" U.S. Patent 6,360,305
8. Stephen T. Novak, Scott Waldron, John C. Peck, Jr., "Queue based memory controller" U.S. Patent 6,295,586
9. Stephen T. Novak, John C. Peck, Jr., Scott Waldron, "Method and apparatus for optimizing memory performance with opportunistic refreshing" U.S. Patent 6,147,921
10. Stephen T. Novak, John C. Peck, Jr., Scott Waldron, "Method and apparatus for optimizing memory performance with opportunistic refreshing" U.S. Patent 6,046,952
11. Stephen T. Novak, Hong-Yi Chen, "Segment descriptor cache for a processor" U.S. Patent 5,926,841
12. Steven Novak, Siyad C. Ma, "Apparatus and methods for native mode processing in a RISC-based CISC processor, U.S. Patent 5,909,567
13. Ian A. Kyles, Ken Kveton, Mike Bourdess, John Wolcott, Steve Novak, Isaac, Gary, "Extremely high frequency systems and methods of operating the same" U.S. Patent 20140273856 A1

**Special Knowledge and Skills**

- FPGAs, ASICs, SoCs, Processors including GPUs, Chipsets
- HDL-Software Interfaces:
    - Programming Language Interface (PLI)
    - SystemVerilog Direct Programming Interface (DPI)
    - Verilog Procedural Interface (VPI)
- Operating systems:
    - Linux
    - UNIX
    - Windows
- Programming languages:

    - C, C++
    - Assembly language, including x86 vector programming
    - Python, including embedded python
    - Perl
    - Java
- Scripting languages
    - Bash
    - Csh
    - Tcl
- Synthesis EDA tools - Synopsys(DC/Primetime/Synplify) , Cadence(Encounter), Xilinx Vivado, Altera Quartus, Magma BlastCreate/Quartzetime
- Simulation EDA tools – Mentor Questa, Synopsys VCS, Cadence Modelsim/Questa, Xilinx Vivado, Altera Quartus
- Logic equivalence EDA tools – Synopsys Formality/LEC
- FPGA development env
    - Xilinx
    - Altera
    - Lattice
- Hardware Description Language
    - Verilog
    - VHDL
    - System Verilog
- Verification methodologies
    - Specman
    - System Verilog
    - Universal Verification Methodology (UVM)