# EDWIN DE ANGEL, Ph.D., P.E.

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## SUMMARY

Dr. De Angel is a professional engineer with more than 25 years of design experience and intellectual property consulting. He holds a Ph.D. in Electrical and Computer Engineering, and is the inventor/co-inventor of more than 30 U.S. patents, and is the author of numerous published articles. Dr. De Angel's work has been paramount in leading mixed-signal ASIC design and development; multimedia technology; wireless technology; memory; parallel processing; power management; embedded systems/DPS and much more for major electronic firms throughout the United States. He has consulted as a subject matter expert in high-profile litigation cases and in the preparation of documents as it pertains to intellectual property matters in his field.

Dr. De Angel is the CEO/founder of Invention Matters LLC, a consulting firm that assists law firms and engineering companies with intellectual property matters. Widely recognized for his work involving asset valuation, claim chart development, prior art research, and patent infringement analysis, he also works as a subject matter expert for technology firms advising on emerging technologies, patent filings, and intellectual property licensing.

Dr. De Angel is fluent in both English and Spanish.

## EDUCATION

**Ph.D. in Electrical and Computer Engineering**
*The University of Texas at Austin* – Austin, Texas - 1996
Dissertation: *Low Power Digital Multiplication*, Supervisor: Dr. Earl E. Swartzlander, Jr.
Related areas: Mobile computing, computer architecture, computer arithmetic, parallel computing, low power technologies, software engineering.

**M.S. in Electrical Engineering**
*Stanford University* – Palo Alto, California - 1992
Key areas: CMOS Analog, Digital VLSI Design, Advanced VLSI, Fast Fourier Transforms, Semiconductor Fabrication, High-Frequency Design, Bipolar Analog Design.

**B.S. in Electrical Engineering**
*University of Puerto Rico* – Mayagüez, Puerto Rico – 1991
Key areas: Digital Electronics, Microprocessors, Digital Systems, Instrumentation, Computer Architecture, Numerical Analysis, Engineering Economics, Accounting, and Economics.

## LICENSES AND PROFESSIONAL AFFILIATIONS

- Professional Engineer, licensed in the state of Texas. License # 84869
- Registered Patent Agent - 82179
- Certified Licensing Professional (CLP)
- Project Management Professional (PMP). Licensed in 2010
- Program Evaluator, ABET (Accreditation Board for Engineering and Technology) 2007-2011
- Institute for Electrical and Electronic Engineering (IEEE) Senior Member
- Tau Beta Pi (Honor Society in Engineering)
- Phi Kappa Phi (National Honor Society)

## LITIGATION CONSULTING EXPERIENCE

**2025 – Segal McCambridge**
**Class Action Lawsuit vs. Sandisk**
U.S. District Court for the Central District of California
3:23-cv-04152-RFL
Represented Sandisk, expected to be deposed in August.

**2024 – Kramer Alberti**
**Polaris PowerLED Technologies, LLC vs. Western Digital Corporation**
U.S. District Court for the Central District of California
2:2024cv02864
Represented Polaris PowerLED Technologies

**2023 – Mintz**
**Daedalus Group LLC vs. Qualcomm**
International Trade Commission
Represented Daedalus Group in two patents related to Power Management: Multiprocessors and Memories

**2022 – Jones Day**
**Impinj, Inc. -v- NXP USA, Inc.**
W. Texas 6:21-CV-00530
Represented NXP and got deposed in two patents related to Power Management/Energy Harvesting

**2017 -- Olavi Dunne, LLP**
**Janus Semiconductor Research, LLC. V. Samsung Austin Semiconductor, LLC.**
Civil Action No. 2:16-CV-01407-JRG-RSP
Represented Janus Semiconductor in patent related to DDR.

**2016 -- Olavi Dunne, LLP**
**Janus Semiconductor Research, LLC. V. SK Hynix, Inc.**
Civil Action No. 2:16-CV-01410-JRG-RSP
Represented Janus Semiconductor in patent related to DDR.

**2016 -- Olavi Dunne, LLP**
**Janus Semiconductor Research, LLC. V. Kingston Technology Company Inc.**
Civil Action No. 2:16-CV-01410-JRG-RSP
Represented Janus Semiconductor in patent related to DDR.

**2016 -- Olavi Dunne, LLP**
**Janus Semiconductor Research, LLC. V. Micron Technology, Inc.**
Civil Action No. 2:16-CV-01410-JRG-RSP
Represented Janus Semiconductor in patent related to DDR.

**2016 -- Texas IP Labs**
**Netlist, Inc. V. SK Hynix Inc.**
Civil Action No. 8:16-cv-01605-JLS-JCG.
Represented Netlist in patents related to DDR memories and SSD.

**2003 -- Jenkins & Gilchrist, LLP**
**Cummins-Allison Corp. V. Glory Inc.**
Civil Action No. 02C 7008
Dispute on the intellectual property of CUMMINS-ALLISON. GLORY INC. is accused of using CUMMINS-ALLISON algorithms in their latest line Money Counter products.

**2002 -- Brobeck, Phleger & Harrison, LLP**
**Alcatel USA, Inc. V. Cisco Systems, Inc.**
Civil Action No. 4:00cv199
Dispute on intellectual property of ALCATEL INC. Intellectual property related to C++ and software defined networks.

## PRESENT ACTIVITIES

**INVENTION MATTERS, LLC (formerly Essential Technologies) -** Austin, Texas
CEO/Founder, 2015-present

Invention Matters, LLC is a consulting firm that provides specialized engineering consulting services to law firms and technology companies in the areas of intellectual property issues, patent infringement analysis, patent valuation, claim chart development, asset valuation, and software issues.

- Pure Storage – External Consultant – Subject Matter Expert (2018 – Present)

- Siipi – External Consultant - Subject Matter Expert (2023)
    - Extensive analysis of Reverse Engineer reports from TechInsights for claim chart development on ASICs of multiple companies (Pre-Litigation work)
    - Team member of reverse engineering team evaluating tools and methodology for a new Reverse Engineering Entity.
- Intellectual Ventures – External Consultant – Subject Matter Expert (2010 – 2018)
    - Extensive analysis of LED lighting, USB/USBC, Buck converter architectures and LED controllers of multiple patent portfolios.
    - Claim chart development on OEMs: USB/USBC, Wi-Fi, Zigbee and other standards.
- Intel Corporation – Subject Matter Expert – (2012 – 2022)
    - Analysis of patent portfolios and strategic patent filing in: circuits, , power converters, power management, Heterogeneous architectures, computer hinges, edge computing. communication peripherals: USB, USBC, HDMI, CAN, and Ethernet
    - Reviewed Reverse Engineer ASIC reports from TechInsights and ScienceVision to identify infringement.
- Texas IP Labs – Subject Matter Expert – (2014 – 2022)
    - Analysis of patent portfolios. Identify ASIC blocks and lead projects requiring reverse engineering working conjuntly with Science Vision.

The firm also provides engineering design and consulting for corporate and legal clients in the areas of systems technology, wireless technology, chip and systems on chip design, power management, embedded systems/DSP, multimedia technologies, and memories.

## RELATED PAST EXPERIENCES

**QUALCOMM –** Austin, Texas 2014

**Low Power Design Consultant**

Low Power Design of multiple power domain Digital Signal Processors:

- Developed system Verilog assertions to test for connectivity of critical low-power signals.
- Analysis and placement of power isolation cells, level shifters, retention cells, and power switches.
- Performed low power verification coverage of digital signal processor:
    - Analyzed and Enhanced UPF power state tables to cover all critical states and transitions.
    - Led the development and implementation of a methodology for power state coverage for digital signal processors using a combination of UVM developed tests, functional vectors, and power-aware assertions.
    - Worked with other verification teams to develop test cases to enhance coverage for retention, power-on reset, and new features added to each core.
- Developed verification test plans

- Performed power-aware simulations:
    - Support debugging of regressions using UPF flow based on VCS/Verdi.
    - Performed RTL modifications to remove always-on buffers: verified modifications using Spyglass and Conformal.
    - Wrote system Verilog assertions and Verilog monitors.

**FREESCALE SEMICONDUCTOR –** Austin, Texas 2013

**Senior Verification Consultant**

Verification of multiple power domain multicore ARM multimedia chip and DRAM controllers/DRAM memory. In charge of:

- low power verification test definition
- Analysis and placement of power isolation cells, retention cells, and power switches.
- Assist in developing and analyzing CPF file
- Developing C language low power test for multiple low power modes, shell scripts, and performing simulation and debugging using Cadence Incisive and Verdi.
- Developed L1/L2 cache tests for boot-up, power-up/down sequences and retention.
- Development of low power checkers in Verilog to track power down/up sequencing, isolation signals
- CPF analysis of level shifters and implementation of low power flow using Cadence Conformal.
- Verification of top-level analog module functionality including Band gaps, PLLs, VCOs, LDOs, DC-DC converter, and multiple clocking modes.

**RFMICRON INC. -** Austin, Texas

VP Engineering, 2009 - 2011

- Defined the design flows, evaluated technology, and selected the team to execute the company's vision.

- Evaluated Intellectual Property from other companies defined licensing terms, technology, and claims analysis.

- Developed and implemented a low-power architecture of Wireless Protocol RFID systems including modeling algorithms in Verilog, coding digital architecture, and implementing level synthesis and top-level simulations. Optimized architecture for power management implementing gated clocks, and multiple voltage domain architecture to meet the extremely low power requirements of the passive RFID tag.

- Defined ASIC design flow and interfaced with Mentor Graphics and Synopsis to implement a full CAD flow to develop and fabricate the chips

- Negotiated fab agreements and evaluate technologies from TSMC, SMIC and UMC. This included mixed signal and flash technologies.

**CIRRUS LOGIC INC. –** Austin, Texas.

Director – System modeling, LED Lighting Division, 2008
- Model LED lighting systems in Mathlab/C language and Hspice.
- Study power efficiency of multiple LED controller architectures

Design Manager and Program Manager, Industrial Product Division, 2006 - 2007

- Led a mixed-signal team of 12 in an 18-month project, implementing the first embedded flash memory, high-performance analog ARM7-based energy measurement ASIC.

- Designed flash memory interface in Verilog and performed top-level system simulations at the transistor level.

- Wrote System Architecture Documents, Technical specifications and led documentation of Test plans, Architecture Reviews, and Design Reviews.

- Implemented LCD/LED display controller for embedded ARM 7 architecture.

Staff Engineer, Embedded Processor Division, 2003 – 2006

- Key member of technical staff in the multimedia product group trusted with the design of critical blocks like video engine, DDR II interface, and new micro controller based architectures for industrial applications, Models developed in C/C++ and implemented in Verilog. Communications peripherals included: USB, HDMI, CAN, Ethernet, I2C, and SPI.

- Led the design of a DDRII memory interface that became a pioneer in the audio/video set-top multimedia market. Designed DLL and simulated the circuit design in Hspice.

- Led architecture and technical specification of microcontroller-based project for industrial applications.

- Implemented LCD/LED display controller for embedded ARM 9 architecture.

**INDEPENDENT CONSULTANT,** Austin, Texas and Chicago, Illinois 2001-2003

Assisted law firms and technology companies as an advisor in intellectual property matters:

- JENKENS & GILCHRIS, LLC – Chicago, Illinois
  Led patent infringement analysis of an electronic sensor system. Performed patent analysis and reverse engineering of the system.

- BROBECK, PHLEGER & HARRISON, LLC – Austin, Texas
  Researched Software of prior art for database systems.
  Prepared expert witnesses and assisted legal team for depositions.
  Developed diagrams and flow charts used in claim charts.

- INFOTRONIC – Austin, Texas
  Reviewed and developed design flow for a processor plus peripherals on a chip.
  Developed contracts with IC vendors and reviewed technical specifications.

**CIRRUS LOGIC INC. – Austin, Texas 1994 - 2001**

Design Manager, Data Acquisition & Audio Division, 1999 - 2001

- Designed and directed a mixed signal system on chip, incorporating ARM7-based processors, Flash memory, Ethernet, and peripherals for industrial applications.

- Researched and recommended a smart sensor architecture integrating high-performance analog, ARM7 processors, and communication peripherals.

- Designed architecture for a low-power bank-based RAM generator used over multiple products of the industrial product division. Simulated critical path and memory cells in Hspice.

Staff Engineer, Data Acquisition Division, 1994 - 1997

- Led low-power architecture for seismic applications. Implemented power management techniques and synthesized digital filters, main controller, and clock generator in Verilog and Synopsys. Conducted design reviews and supervised layout and tape-out of chips.
- Designed DC-DC converter, simulated circuit design in Hspice/Smartspice and supervise layout and fabrication.
- Designed Low power ROM. Simulated circuit design in Hspice/Smartspice and supervised layout.
- Performed characterization of ASICs, decapping and probing chips.

**HONEYWELL CORP. – Phonix, AZ 1991, 1992 (Summers)**

- Layout and Circuit design implementation of LED drivers in CMOS/NMOS. This technology was the pioneer technology that went into the LED displays of the Boeing 777.

## PATENTS

"**Method and Apparatus for Detecting RF Field Strength**," Shahriar Rokhsaz, Edwin De Angel, U.S. Patent Pending

"**Method and Apparatus for Authenticating RFID tags**," Shahriar Rokhsaz, Edwin De Angel, U.S. Patent Pending

"**Complex Wavelet Filter Based Power Measurement and Calibration System**," Dale Brummel, Hang Liu, Robert Leon Gorsegner, Edwin De Angel, Jean Charles Pina, U.S. Patent 8165835

"**Method and Apparatus for Automatically Securing Non-Volatile (NV) Storage in an Integrated Circuit**," Edwin De Angel, Jorge Antonio Abullarade, Jean Charles Pina, Rahul Singh, U.S. Patent 7657722

"**Method and Apparatus for Reducing Switching Noise in a System-On-Chip (SoC) Integrated Circuit Including an Analog-to-Digital Converter (ADC)**," Rahul Singh, Prashanth Drakshapalli, Jie Fang, Edwin De Angel, Mohit Sood, U.S. Patent 7515076

"**Integrated Circuit with Mode Control for Selecting Settled and Unsettled Output from a Filter**," Axel Thomsen, Jerome E. Johnston, Edwin De Angel, Aryesh Amar, U.S. Patent 7162506

"**Sinc Filter Using Twisting Symmetry**," Joel Page, Edwin De Angel, Wai Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow, U.S. Patent 6546408

"**Application of a Conditionally Stable Instrumentation Amplifier to Industrial Measurement**," Axel Thomsen, Edwin De Angel, Sherry Wu, Aryesh Amar, Jerome E. Johnston U.S. Patent 6525589

"**Independent Control of Calibration Registers in a Multi Channel A-D converter**" Aryesh Amar, Edwin De Angel, Eric J. Swanson U.S. Patent 6426713

"**System and Techniques for Seisimic Data Acquisition,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6337636

"**Linear Phase FIR Sinc Filter with Multiplexing,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6321246

"**Sinc Filter with Selective Decimation Ratios,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6317765

"**Noise Management Using A Switched Converter**," Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6281718

"**Noise Invariant Circuits, Systems and Methods**," Edwin De Angel, Eric J. Swanson U.S. Patent 6901423

"**Correct Carry Bit Generation,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6243733

"**Multiplier Sign Extension,**" Edwin De Angel U.S. Patent 6183122

"**Techniques for Signal Measurement using a Conditionally Stable Amplifier,**" Axel Thomsen, Edwin De Angel, Sherry Wu, Lei Wang, Aryesh Amar U.S. Patent 6891430

"**Independent Control of Calibration Registers in a Multi Channel A-D Converter**," Aryesh Amar, Edwin De Angel, Eric J. Swanson U.S. Patent 6426713

"**Digital Multiplier with Multiplier Encoding Involving a 3X Term,**" Edwin De Angel U.S. Patent 6085214

"**Ultra Low Power Multiplier,**" Edwin De Angel U.S. Patent 5787029

"**Network Synchronization,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 7218612

"**Power on reset techniques for an integrated circuit chip,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow U.S. Patent 6980037

"**Clock Alignment for Reduced Noise and Easy Interfacing,**" Joel Page, Edwin De Angel, Wai Laing Lee, Lei Wang, Hong Helena Zheng, Chung-Kai Chow –U.S. Patent 9153861

"**Multiplier Power Saving Design,**" Edwin De Angel U.S. Patent 6604120

## PUBLICATIONS

"**Switching Activity in Parallel Multipliers,**" Edwin de Angel and Earl E. Swartzlander Jr., 2001 Asilomar Conference

"**Survey of Low Power Techniques for Parallel Multipliers,**" Edwin de Angel and Earl E. Swartzlander Jr., Newsletter *in Transactions on VLSI Systems,* spring 2000

"**A DC measurement IC with 130nVpp noise in 10Hz using a 4-stage chopper stabilized CMOS instrumentation amplifier**," Axel Thomsen, Edwin de Angel, Sherry Xiaohong Wu, Aryesh Amar, Lei Wang, Wai Lee, *2000 International Solid State Circuits Conference pp 334-335.*

"**24 by 24 Multiplier Using a Carry Propagate Radix-4 Encoding Scheme,**" Edwin de Angel, Eric Swanson and Wai Lee, paper submitted to *1999 International Symposium on Signals, Circuits, and Systems.*

"**A Survey of Low Power Techniques for ROMs**", Edwin de Angel and Earl E. Swartzlander Jr., *1997 International Symposium on Low Power Electronics*, pp. 7-11.

"**Low Power Parallel Multipliers**," Edwin de Angel and Earl E. Swartzlander Jr., *1996 VLSI Signal Processing,* pp. 199-208.

Chapter "**Low Power Digital Multipliers**," Edwin de Angel, published in *Application Specific Processors*, Kluwer Academic Publishers. pp. 91-114.

"**A Survey of Low Power Techniques for VLSI**," Edwin de Angel and Earl E. Swartzlander Jr., *1996 Innovative Systems on Silicon,* pp. 159-169.

"**An Ultra Low Power Multiplier**," Edwin de Angel and Earl E. Swartzlander Jr., *1995 International Conference in Signal Processing and Applications*, pp. 2118-2122.

"**The Star Multiplier**," Edwin de Angel, Andalib Chowdury and Earl E. Swartzlander Jr., *1995 Asilomar Conference,* pp. 604-607.

"**A New Asynchronous Multiplier,**" Edwin de Angel, Jacob Abraham and Earl E. Swartzlander Jr., *1994 International Conference on Computer Design,* pp. 302-305.